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(71) Applicant: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.**
Atsugi-shi Kanagawa-ken 243-0036 (JP)

(72) Inventors:
- **Ohtani, Hisashi**
  Isehara-shi, Kanagawa-ken 259-11 (JP)
- **Miyanaga, Akiharu**
  Hadano-shi, Kanagawa-ken 257 (JP)
- **Fukunaga, Takeshi**
  Atsugi-shi, Kanagawa-ken 243 (JP)
- **Zhang, Hongyong**
  Yamato-shi, Kanagawa-ken 243 (JP)

(74) Representative: **Milhench, Howard Leslie et al**
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

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(54) Method of crystallizing a silicon layer

(57) A process for fabricating a highly stable and reliable semiconductor, comprising: coating the surface of an amorphous silicon film with a solution containing a catalyst element capable of accelerating the crystallization of the amorphous silicon film, and heat treating the amorphous silicon film thereafter to crystallize the film.

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Description

BACKGROUND OF THE INVENTION

[Field of the Invention]

[0001] The present invention relates to a process for manufacturing a semiconductor device having a crystalline semiconductor. The present invention further relates to an electro-optical device such as an active matrix liquid crystal device using the semiconductor device.

[Prior Art]

[0002] Thin film transistors (referred to simply hereinafter as "TFTs") are well known and are widely used in various types of integrated circuits or an electro-optical device, and particularly used for switching elements provided to each of pixels of an active matrix(-addressed) liquid crystal display device as well as in driver elements of the peripheral circuits thereof.

[0003] An amorphous silicon film can be utilized most readily as the thin film semiconductor for a TFT. However, the electric characteristics of the amorphous silicon film are disadvantageously poor. The use of a thin film of polysilicon (polycrystalline silicon), which is a crystalline silicon, can solve the problem. Crystalline silicon is denoted as, for example, polycrystalline silicon, polysilicon, and microcrystalline silicon. The crystalline silicon film can be prepared by first forming an amorphous silicon film, and then heat treating the resulting film for crystallization.

[0004] The heat treatment for the crystallization of the amorphous silicon film requires heating the film at a temperature of 600 °C or higher for a duration of 10 hours or longer. Such a heat treatment is detrimental for a glass substrate. For instance, a Corning 7059 glass commonly used for the substrate of active matrix liquid crystal display devices has a glass distortion point of 593 °C, and is therefore not suitable for large area substrates that are subjected to heating at a temperature of 600 °C or higher.

[0005] According to the study of the present inventors, it was found that the crystallization of an amorphous silicon film can be effected by heating the film at 550 °C for a duration of about 4 hours. This can be accomplished by disposing a trace amount of nickel or palladium, or other elements such as lead, onto the surface of the amorphous silicon film.

[0006] The elements above (hereinafter referred to as "catalyst elements capable of accelerating the crystallization of an amorphous silicon film" or simply as "catalyst elements") can be introduced into the surface of the amorphous silicon film by depositing the elements by plasma treatment or vapor deposition, or by incorporating the elements by ion implantation. The plasma treatment more specifically comprises adding the catalyst elements into the amorphous silicon film by generating a plasma in an atmosphere such as gaseous hydrogen or nitrogen using an electrode containing catalyst elements therein in a plasma CVD apparatus of a parallel plate type or positive columnar type.

[0007] However, the presence of the catalyst elements in a large quantity in the semiconductor is not preferred, because the use of such semiconductors greatly impairs the reliability and the electric stability of the device in which the semiconductor is used.

[0008] That is, the catalyst elements are necessary in the crystallization of the amorphous silicon film, but are preferably not incorporated in the crystallized silicon. These conflicting requirements can be accomplished by selecting an element which tend to be inactive in crystalline silicon as the catalyst element, and by incorporating the catalyst element at a minimum amount possible for the crystallization of the film. Accordingly, the quantity of the catalyst element to be incorporated in the film must be controlled with high precision.

[0009] The crystallization process using nickel or the like was studied in detail. The following findings were obtained as a result:

(1) In case of incorporating nickel by plasma treatment into an amorphous silicon film, nickel is found to intrude into the film to a considerable depth of the amorphous silicon film before subjecting the film to a heat treatment;
(2) The initial nucleation occurs from the surface from which nickel is incorporated; and
(3) When a nickel layer is deposited on the amorphous silicon film, the crystallization of an amorphous silicon film occurs in the same manner as in the case of effecting plasma treatment.

[0010] In view of the foregoing, it is assumed that not all of the nickel introduced by the plasma treatment functions to promote the crystallization of silicon. That is, if a large amount of nickel is introduced, there exists an excess amount of the nickel which does not function effectively. For this reason, the inventors consider that it is a point or face at which the nickel contacts the silicon that functions to promote the crystallization of the silicon at lower temperatures. Further, it is assumed that the nickel has to be dispersed in the silicon in the form of atoms. Namely, it is assumed that nickel needs to be dispersed in the vicinity of a surface of an amorphous silicon film in the form of atoms, and the concentration of the nickel should be as small as possible but within a range which is sufficiently high to promote the low temperature crystallization.

[0011] A trace amount of nickel, i.e., a catalyst element capable of accelerating the crystallization of the amorphous silicon, can be incorporated in the vicinity of the surface of the amorphous silicon film by, for example, vapor deposition. However, vapor deposition is disadvantageous concerning the controllability of the film, and is therefore not suitable for precisely controlling the

amount of the catalyst element to be incorporated in the amorphous silicon film.

SUMMARY OF THE INVENTION

[0012] In the light of the aforementioned circumstances, the present invention aims to fabricate with high productivity, a thin film of crystalline silicon semiconductor by a heat treatment at a relatively low temperature using a catalyst element, provided that the catalyst element is incorporated by precisely controlling the quantity thereof.

[0013] In accordance with one aspect of the present invention, the foregoing objects can be achieved by providing an amorphous silicon film with a catalytic element for promoting the crystallization thereof or a compound including the catalytic element in contact with the amorphous silicon film. and heat treating the amorphous silicon with said catalytic element or said compound being in contact therewith, thereby, the silicon film is crystallized.

[0014] Preferably but not essentially, a solution containing the catalytic element is provided in contact with an amorphous silicon film in order to introduce the catalytic element into the amorphous silicon film.

[0015] According to a second aspect of the present invention there is provided a method of manufacturing a semiconductor device comprising addingamaterial selected from the group consisting of Ni, Pd, Pt, Cu, Ag, Au, In, Sn, Pd, Sn, P, As and Sb into a silicon semiconductor film or a portion thereof at a trace amount by contacting a solution containing said material with the silicon film and then crystallize the silicon semiconductor film by heating at a relatively low temperature.

[0016] According to a third aspect of the present invention there is provided a method for manufacturing a semiconductor device comprising the steps of: adding a crystallization promoting material into a first region of a silicon film formed on a surface, by disposing a solution containing said crystallization promoting material in contact with a selected portion of the silicon film; and heating said silicon film in order that crystals grow from said first region toward a second region of the silicon film to which said crystallization promoting material is not directly added.

[0017] According to a fourth aspect of the present invention there is provided a method of manufacturing a semiconductor device comprising:preparing a solution containing a compound dissolved or dispersed in a polar or non-polar solvent, the compound including a crystallization promoting material; disposing the solution in contact with a silicon film and crystallizing said silicon film by heating.

[0018] The present invention also extends to a semiconductor device having at least an active region comprising crystalline silicon and to a method of manufacturing an insulated gate field effect semiconductor device. Examples of how these devices can be manufactured are described in the following description but it should be noted that the invention is not limited to the methods described therein, i.e. the invention is not limited to providing a catalyst for promoting crystallisation or to providing the catalyst by way of a solution.

[0019] Therefore according to a fifth aspect of the present invention there is provided a method for manufacturing an insulated gate field effect semiconductor device comprising the steps of: forming an amorphous silicon film on an insulating surface; crystallizing said silicon film; and oxidizing a surface of said silicon film in an oxidizing atmosphere containing water vapor in order to form a gate insulating film.

[0020] In addition, even if a catalyst is used to obtain a semiconductor device having an active region of crystalline silicon, the active region may comprise crystalline silicon which does not contain any catalyst as it has been grown away from its region of seeding. Such a semiconductor device is novel and could still be readily identified by examination of its crystalline planes even if the region which was catalysed subsequently has been removed. Therefore, according to a sixth embodiment of the invention there is provided a semiconductor device including at least an active region comprising crystalline silicon formed on a substrate, wherein a surface of said silicon film has at least one of planes {111}, those expressed by {hk1} (h+k=1), and a neighborhood thereof.

[0021] Furthermore, according to a seventh embodiment of the present invention there is provided a method of manufacturing a semiconductor device, said method comprising seeding a first region of a silicon substrate and heating said substrate to grow crystals laterally from said first region to a second region of said silicon substrate.

[0022] By utilizing the silicon film having a crystallinity thus formed, it is possible to form an active region including therein at least one electric junction such as PN, PI or NI junction. Examples of semiconductor devices are thin film transistors (TFT), diodes, photo sensor, etc.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The foregoing objects and features of the present invention will be described in detail with reference to the attached figures in which:

Figs. 1A to 1D are cross sectional views for forming a crystalline silicon film in accordance with the present invention;

Figs. 2A and 2B are cross sectional views showing a formation of a crystalline silicon film in accordance with the present invention;

Fig. 3 is a graph showing a relation of a lateral growth length of crystals with respect to a concentration of nickel in a solution;

Fig. 4 is a graph showing a SIMS data with respect to nickel in a silicon region into which nickel is di-

rectly added;
Fig. 5 is a graph showing a SIMS data with respect to nickel in a silicon region where crystals grow along the lateral direction from the region into which nickel is directly added;
Figs. 6A to 6E show cross sectional views showing a manufacturing process of a semiconductor device in accordance with Example 3 of the present invention;
Fig. 7 shows a Ni concentration in a silicon film subjected to a plasma treatment;
Fig. 8 is a Raman spectroscopic diagram with respect to a region into which nickel is directly added;
Fig. 9 is a Raman spectroscopic diagram with respect to a region where crystals grow in a lateral direction;
Figs. 10A-10F are cross sectional views showing a manufacturing process of an electro-optical device in accordance with Example 4 of the present invention.
Figs. 11A-11D are cross sectional views showing a manufacturing process of a TFT in accordance with Example 5 of the present invention;
Fig. 12 shows a schematic diagram of an active matrix type electro-optical device in accordance with Example 6 of the present invention;
Figs. 13A and 13B are cross sectional views showing the formation of a crystalline silicon film in accordance with Example 7 of the present invention;
Figs. 14A-14E are cross sectional views showing a manufacturing process of a TFT in accordance with Example 8 of the present invention; and
Figs. 15A and 15B are schematic diagrams showing an arrangement of an active layer of a TFT in accordance with Example 8 of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0024] The use of a solution for adding nickel or the like according to the present invention is advantageous in the following points:

(a) The concentration of the catalyst element (e.g. nickel) in the solution can be accurately controlled in advance;
(b) The amount of the catalyst element incorporated into the amorphous silicon film can be determined by the concentration of the catalyst element in the solution so long as the surface of the amorphous silicon film is brought into contact with the solution; and
(c) The catalyst element can be incorporated at a minimum concentration necessary for the crystallization into the amorphous silicon film, because the catalyst element adsorbed by the surface of the amorphous silicon film principally contributes to the crystallization of the film.

[0025] The word "including" or "containing" mentioned in the present specification may be understood as either (a) that the catalytic element is simply dispersed in a solution or (b) that the catalytic element is contained in a solution in a form of a compound. As a solution, various aqueous solutions and organic solvent solutions can be used. Those solvents can be roughly classified into a polar solvent and a non-polar solvent.

[0026] Water, alcohol, acid or ammonium can be used as a polar solvent. Examples of nickel compounds which are suitable for the polar solvent are nickel bromide, nickel acetate, nickel oxalate, nickel carbonate, nickel chloride, nickel iodide, nickel nitrate, nickel sulfate, nickel formate, nickel acetyl acetonate, 4-cyclohexyl butyric acid, nickel oxide and nickel hydroxide.

[0027] Also, benzene, toluene, xylene, carbon tetrachloride, chloroform or ether can be used as a non-polar solvent. Examples of nickel compounds suitable for a non-polar solvent are nickel acetyl acetonate and 2-ethyl hexanoic acid nickel.

[0028] Further, it is possible to add an interfacial active agent to a solution containing a catalytic element. By doing so, the solution can be adhered to and adsorbed by a surface at a higher efficiency. The interfacial active agent may be coated on the surface to be coated in advance of coating the solution.

[0029] Also, when using an elemental nickel (metal), it is necessary to use an acid to dissolve it.

[0030] In the foregoing examples, the nickel can be completely solved by the solvent. However, even if the nickel is not completely solved, it is possible to use a material such as an emulsion in which elemental nickel or nickel compound is dispersed uniformly in a dispersion medium.

[0031] When using a polar solvent such as water for dissolving nickel, it is likely that an amorphous silicon film repels such a solution. In such a case, a thin oxide film is preferably formed on the amorphous silicon film so that the solution can be provided thereon uniformly. The thickness of the oxide film is preferably 100 Å or less. Also, it is possible to add an interfacial active agent to the solution in order to increase a wetting property.

[0032] Further, it is possible to conduct a rubbing treatment on the surface of the thin oxide film in order to give the surface an irregularity with a uniform gap, width and direction. Such irregularity helps the solvent to permeate, thereby, increasing the uniformity of the size and directions of crystal grains. Also, such a crystalline semiconductor film in which crystals are oriented in a particular direction is advantageous to be used for a semiconductor device in order to increase a uniformity of device characteristics.

[0033] Also, when using a non-polar solvent such as toluene for obtaining a solution of 2-ethyl hexanoic acid nickel, the solution can be directly formed on the surface of an amorphous silicon film. However, it is possible to interpose between the amorphous silicon film and the solution a material for increasing the adhesivity there-

between, for example, OAP (containing hexamethyl disilazane as a main component, produced by Tokyo Oka Kogyo) which is used to increase adhesivity of a resist.

[0034] The concentration of the catalyst element in the solution depends on the kind of the solution, however, roughly speaking, the concentration of the catalyst element such as nickel by weight in the solution is 1 ppm to 200 ppm, and preferably, 1 ppm to 50 ppm, and more preferably 10 ppm or lower. The concentration is determined based on the nickel concentration in the silicon film or the resistance against hydrofluoric acid of the film upon completion of the crystallization.

[0035] The crystal growth can be controlled by applying the solution containing the catalyst element to a selected portion of the amorphous silicon film. In particular, the crystals can be grown in the silicon film by heating the silicon film in a direction approximately parallel with the plane of the silicon film from the region onto which the solution is directly applied toward the region onto which the solution is not applied.

[0036] It is also confirmed that this lateral growth region contains the catalyst element at a lower concentration. It is useful to utilize a crystalline silicon film as an active layer region for a semiconductor device, however, in general, the concentration of the impurity in the active region is preferably as low as possible. Accordingly, the use of the lateral growth region for the active layer region is useful in device fabrication.

[0037] The use of nickel as the catalyst element is particularly effective in the process according to the present invention. However, other useful catalyst elements include nickel (Ni), palladium (Pd), platinum (Pt), copper (Cu), silver (Ag), gold (Au), indium (In), tin (Sn), phosphorus (P), arsenic (As), and antimony (Sb). Otherwise, the catalyst element may be at least one selected from the elements belonging to the Group VIII, IIIb, IVb, and Vb of the periodic table.

EXAMPLE 1

[0038] The present example refers to a process for fabricating a crystalline silicon film on the surface of a glass substrate. Referring to Figs. 1A-1D, the process for incorporating a catalyst element (nickel in this case) into the amorphous silicon film is described below. A Corning 7059 glass substrate 100 mm x 100 mm in size is used.

[0039] An amorphous silicon film from 100 to 1,500 Å in thickness is deposited by plasma CVD or LPCVD. More specifically in this case, an amorphous silicon film 12 is deposited at a thickness of 1,000 Å by plasma CVD (Fig. 1A).

[0040] Then, the amorphous silicon film is subjected to hydrofluoric acid treatment to remove impurities and a natural oxide formed thereon, if necessary. This treatment is followed by the deposition of an oxide film 13 on the amorphous silicon film to a thickness of from 10 to 50 Å. A natural oxide film may be utilized as the oxide film. The precise thickness of the oxide film 13 is not available because the film is extremely thin. However, the natural oxide film is assumably about 20 Å in thickness. The oxide film 13 is deposited by irradiating an ultraviolet (UV) radiation in an oxygen atmosphere for a duration of 5 minutes. The oxide film 13 can be formed otherwise by thermal oxidation. Furthermore, the oxide film can be formed by a treatment using aqueous hydrogen peroxide.

[0041] The oxide film 13 is provided with an aim to fully spread the acetate solution containing nickel, which is to be applied in the later step, on the entire surface of the amorphous silicon film. More briefly, the oxide film 13 is provided for improving the wettability of the amorphous silicon film. If the aqueous acetate solution were to be applied directly, for instance, the amorphous silicon film would repel the aqueous acetate solution to prevent nickel from being incorporated uniformly into the surface of the amorphous silicon film.

[0042] An aqueous acetate solution containing nickel added therein is prepared thereafter. More specifically, an aqueous acetate solution containing nickel at a concentration of 10 to 200 ppm, e.g. 100 ppm, is prepared. Two milliliters of the resulting acetate solution is dropped to the surface of the oxide film 13 on the amorphous silicon film 12, and is maintained as it is for a predetermined duration of time, preferably for a duration of 0.5 minutes or longer, e.g. for a duration of 5 minutes. Spin drying at 2,000 rpm using a spinner is effected for 60 seconds thereafter to remove the unnecessary solution (Figs. 1C and 1D).

[0043] The concentration of nickel in the acetate solution is practically 1 ppm or more, preferably, 10 ppm or higher. The solution needs not be only an acetate solution, and other applicable solutions include those of hydrochlorides, nitrates, and sulfates. Otherwise, those of organic octylates and toluene can be used as well. In case of using the organic solutions, the oxide film 13 need not be incorporated because the solution can be directly applied to the amorphous silicon film to introduce the catalyst elements into the film.

[0044] The coating of the solution is carried out at one time or may be repeated, thereby, it is possible to form a film containing nickel on the surface of the amorphous silicon film 12 uniformly to a thickness of several angstrom to several hundreds angstrom after the spin dry. The nickel contained in this film will diffuse into the amorphous silicon film during a heating process carried out later and will function to promote the crystallization of the amorphous silicon film. By the way, it is the inventors' intention that the film containing nickel or other materials do not necessarily have to be in the form of a completely continuous film, that is, it may be discontinuous, for example, in the form of number of clusters.

[0045] The amorphous silicon film coated with one of the above solutions is kept as it is thereafter for a duration of 5 minutes. The final concentration of nickel catalyst element in the crystallized silicon film 12 can be

controlled by changing this retention time, however, the most influencing factor in controlling the final concentration of nickel catalyst element in the crystallized silicon film is the concentration of the nickel catalyst element in the solution.

[0046] The silicon film coated with a nickel-containing solution thus obtained is subjected to heat treatment at a temperature of 550 °C for a duration of 4 hours in a nitrogen atmosphere in a heating furnace. Thus, a thin film of crystalline silicon 12 is formed on the substrate 11.

[0047] The heat treatment can be effected at any temperature of 450 °C or higher. If a low temperature is selected, however, the heat treatment would consume much time and result in a poor production efficiency. If a heat treatment temperature of 550 °C or higher were to be selected, on the other hand, the problem of heat resistance of the glass substrate must be considered.

EXAMPLE 2

[0048] The present example refers to a process similar to that described in Example 1, except that a silicon oxide film 1,200 Å in thickness is provided selectively to incorporate nickel into selected regions of the amorphous silicon film using the silicon oxide film as a mask.

[0049] Referring to Figs. 2A to 2C, the process for fabricating a semiconductor according to the present example is described below. A silicon oxide film is deposited to a thickness of 1,000 Å or more e.g. 1200 Å as a mask on an amorphous silicon film 12. The silicon oxide film 21, however, may be thinner than 1000 Å, e.g. 500 Å if the film is sufficiently dense as a mask. The silicon oxide film 21 is patterned into a predetermined pattern thereafter by means of a conventional photolithography technique. A thin silicon oxide film 20 is formed by irradiating a UV radiation in oxygen atmosphere for 5 minutes. The thickness of the silicon oxide film 20 is presumably from about 20 to 50 Å (Fig. 2A). The function of the silicon oxide film thus formed for improving the wettability of the amorphous silicon film might be occasionally provided by the hydrophilic nature of the silicon oxide film formed as the mask in case the solution is matched with the size of the mask pattern. However, this is a special case, and, in general, a silicon oxide film 20 is safely used.

[0050] Then, similar to the process described in Example 1, 5 milliliters (with respect to a substrate 10 cm x 10 cm in size) of an acetate solution containing 100 ppm of nickel is dropped to the surface of the resulting structure. A uniform aqueous film is formed on the entire surface of the substrate by effecting spin coating using a spinner at 50 rpm for a duration of 10 seconds. Then, after maintaining the state for a duration of 5 minutes, the resulting structure is subjected to spin drying using a spinner at a rate of 2,000 rpm for a duration of 60 seconds. During the retention time, the substrate may be rotated on the spinner at a rate of 100 rpm or lower (Fig. 2B).

[0051] The amorphous silicon film 12 is crystallized thereafter by applying heat treatment at 550 °C for a duration of 4 hours in gaseous nitrogen. It can be seen that the crystal growth proceeds along a lateral direction from the region 22 into which nickel is introduced as shown by arrow 23 toward the region 25 into which nickel is not directly introduced.

[0052] In Fig. 2C, the reference numeral 24 shows a region in which the nickel is directly introduced to cause the crystallization and the reference numeral 25 shows a region in which the crystallization proceeds laterally from the region 24.

[0053] It was confirmed through transmission electron microscopy (TEM) and electron diffraction that:

(a) the crystals grown in a lateral direction are monocrystalline in the form of needle or column having uniform widths;
(b) the growth direction of the crystals are approximately parallel with the substrate surface although it depends upon the film thickness; and
(c) the growth direction of the crystals are substantially aligned with the [111] axis of the crystals.

[0054] From the foregoing facts, it can be concluded that the surface of the lateral growth region 25 has a plane which is at least one of those expressed by {hk1} (h+k=1), for example, {110}, {123}, {134}, {235}, {145}, {156}, {257}, or {167}, or the neighborhood thereof.

[0055] It should be noted that since crystalline silicon has a diamond structure of which space group is indicated by Fd3m, when the above index hk1 is even-odd mixing, a forbidden reflection occurs and it can not be observed with the electron diffraction.

[0056] Fig. 3 shows the relation between the distance (μm) of the crystal growth to the region 23 along the transverse (lateral) direction and the nickel concentration (ppm) in the aqueous acetate solution.

[0057] Fig. 3 reads that a crystal growth for a distance of 25 μm or longer can be realized by preparing a solution containing nickel at a concentration of 100 ppm or higher. It can be also assumed from Fig. 3 that a crystal growth along the lateral direction of about 10 μm can be obtained by using an aqueous acetate solution containing nickel at a concentration of 10 ppm.

[0058] The datum plotted in Fig. 3 are for the case that the structure was held for a duration of 5 minutes after applying the nickel-containing aqueous acetate solution. However, the distance of crystal growth along the lateral direction changes with the retention time.

[0059] In case of using an aqueous acetate solution containing nickel at a concentration of 100 ppm, for instance, longer distance of crystal growth can be obtained with increasing retention time up to 1 minute. However, once a retention time of 1 minute or longer is set, the further increase becomes insignificant.

[0060] In case an aqueous acetate solution contain-

ing nickel at a concentration of 50 ppm is used, the retention time increases proportional to the distance of the crystal growth along the lateral direction. However, the increment tends to saturate with increasing retention time to 5 minutes or longer.

[0061] Furthermore, it should be noted that temperature greatly influences the time necessary for a reaction to achieve an equilibrium. Accordingly, the retention time is also subject to the temperature, and a strict control of the temperature is indispensable. Thus, the distance of crystal growth can be increased in total by elevating the temperature of heat treatment and by elongating the duration of the heat treatment.

[0062] Figs. 4 and 5 show the nickel concentration in a silicon film obtained by introducing nickel using an aqueous acetate solution containing 100 ppm nickel and thereafter heat treating the silicon film at 550 °C for a duration of 4 hours. The nickel concentration is obtained by secondary ion mass spectroscopy (SIMS).

[0063] Fig. 4 shows the nickel concentration of the region 24 shown in Fig. 2C, i.e., the region into which nickel is directly incorporated. Fig. 5 shows the nickel concentration of the region 25 in Fig. 2C, i.e., the region in which crystal growth occurred along the lateral direction from the region 22.

[0064] By comparing the data of Fig. 4 with that of Fig. 5, it can be seen that the nickel concentration of the region in which the crystal growth occurs along the lateral direction is lower by about one digit as compared with that of the region into which nickel is introduced directly.

[0065] It can be seen also that the nickel concentration in the crystallized silicon film in the region into which nickel is introduced directly can be suppressed to a level of 10^{18} cm^{-3} by using an aqueous acetate solution containing nickel at a concentration of 10 ppm.

[0066] Conclusively, it is understood that the nickel concentration in the crystalline silicon region in which the crystal growth occurs along the lateral direction can be suppressed to 10^{17} cm^{-3} or lower by using an aqueous acetate solution containing nickel at a concentration of 10 ppm and effecting the heat treatment at 550 °C or higher for a duration of 4 hours or longer.

[0067] In conclusion, it is possible to control the concentration of nickel in the region 24 of the silicon film where the nickel is directly added within a range of 1×10^{16} atoms/cm^3 to 1×10^{19} atoms/cm^3 by controlling the density of the solution and the retention time and further to maintain the concentration of the nickel in the lateral growth region 25 below that.

[0068] For comparison, a sample is prepared through a process in which, instead of using a nickel containing solution, an amorphous silicon film is exposed to a plasma which is produced by using an electrode containing an amount of nickel in order to add the nickel into the silicon (this is called as a plasma treatment), and further the silicon film is crystallized by a heat annealing at 550 °C for 4 hours. The condition of the plasma treatment is selected so that the same degree of a lateral crystal growth can be obtained as in the case where an acetic acid containing nickel at 100 ppm is used. The SIMS data with respect to this sample is shown in Fig. 7. As can be seen, in the case of using a plasma treatment, the nickel concentration in the lateral growth region is higher than 5×10^{18} atoms/cm^3 which is undesirably high for an active region of a semiconductor device. Accordingly, it is to be understood that the use of a solution is advantageous for minimizing the concentration of the nickel in the lateral growth region.

[0069] Fig. 8 shows a result of Raman spectroscopy with respect to the region corresponding to Fig. 4, namely, the region where the nickel is directly introduced. Fig. 8 indicates that the crystallinity in this region is extremely high. Also, Fig. 9 shows a result of Raman spectroscopy with respect to the region where the crystal grows laterally. As can be seen, even in the lateral growth area, the intensity of the Raman spectrum is more than 1/3 of the intensity of the single crystal silicon. Accordingly, it is concluded that the crystallinity in the lateral growth region is also high.

[0070] The crystalline silicon film thus fabricated by the process according to the present invention is characterized in that it exhibits an excellent resistance against hydrofluoric acid. To the present inventors' knowledge, if the nickel is introduced by a plasma treatment, the resistivity of the crystallized silicon against a hydrofluoric acid is poor. When it is necessary to pattern a silicon oxide film which is formed over the crystalline silicon film for forming a contact hole therethrough, a hydrofluoric acid is usually used as an etchant. If the crystalline silicon film has a sufficiently high resistance against the hydrofluoric acid, a large selection ratio (the difference in the etching rate of the silicon oxide film and the crystalline silicon film) can be objected so as to remove the silicon oxide film alone. Accordingly, a crystalline silicon film having high resistance against attack of hydrofluoric acid is of great advantage in the fabrication process of a semiconductor device.

EXAMPLE 3

[0071] The present example relates to a process for fabricating TFTs which are provided to each of the pixels of an active matrix liquid crystal display device, using a crystalline silicon film fabricated by the process according to the present invention. The TFTs thus obtained can be applied not only to liquid crystal display devices, but also to a wide field generally denoted as thin film integrated circuits (ICs).

[0072] Referring to Figs. 6A to 6E, the process for fabricating a TFT according to the present example is described below. A silicon oxide film (not shown in the figure) is deposited to a thickness of 2,000 Å as a base coating on a glass substrate. This silicon oxide film is provided to prevent the diffusion of impurities into the device structure from the glass substrate.

[0073] An amorphous silicon film is deposited there-

after to a thickness of 1,000 Å in a manner similar to that used in Example 1. After removing the natural oxide film by a treatment using hydrofluoric acid, a thin film of an oxide film is formed to a thickness of about 20 Å by means of UV irradiation under a gaseous oxygen atmosphere.

[0074] The resulting amorphous silicon film having the oxide film thereon is coated with an aqueous acetate solution containing nickel at a concentration of 10 ppm. The resulting structure is retained for a duration of 5 minutes, and is subjected thereafter to spin drying using a spinner. The silicon oxide film is removed thereafter using a buferred hydrofluoric acid, and a silicon film is crystallized by heating the resulting structure at 550 °C for a duration of 4 hours. The process up to this step is the same as that described in Example 1.

[0075] The silicon film thus crystallized is patterned to form an island-like region 104 as shown in Fig. 6A. The island-like region 104 provides the active layer for the TFT. A silicon oxide film 105 is formed thereafter for a thickness of from 200 to 1,500 Å at a thickness of 1,000 Å. The silicon oxide film functions as a gate insulating film (Fig. 6A).

[0076] The silicon oxide film 105 is deposited by means of RF plasma CVD process using TEOS (tetraethoxysilane). That is, TEOS is decomposed and then deposited together with oxygen at a substrate temperature of 150 to 600 °C, preferably in the range of 300 to 450 °C. TEOS and oxygen are introduced at a pressure ratio of 1:1 to 1:3 under a total pressure of 0.05 to 0.5 Torr, while applying an RF power of 100 to 250 W. Otherwise, the silicon oxide film can be fabricated by reduced pressure CVD or normal pressure CVD using TEOS as the starting gas together with gaseous ozone, while maintaining the substrate temperature in the range of from 350 to 600 °C, preferably, in the range of from 400 to 550 °C. The film thus deposited is annealed in oxygen or under ozone in the temperature range from 400 to 600 °C for a duration of from 30 to 60 minutes.

[0077] The crystallization of the silicon region 104 can be accelerated by irradiating a laser beam using a KrF excimer laser (operating at a wavelength of 248 nm at a pulse width of 20 nsec) or an intense light equivalent thereto. The application of RTA (rapid thermal annealing) using infrared radiation is particularly effective because the silicon film can be heated selectively without heating the glass substrate. Moreover, RTA is especially useful in the fabrication of insulated gate field effect semiconductor devices because it decreases the interface level between the silicon layer and the silicon oxide film.

[0078] Subsequently, an aluminum film is deposited to a thickness of from 2,000 Å to 1 μm by electron beam vapor deposition, and is patterned to form a gate electrode 106. The aluminum film may contain from 0.15 to 0.2 % by weight of scandium as a dopant. The substrate is then immersed into an ethylene glycol solution controlled to a pH of about 7 and containing 1 to 3% tartaric acid to effect anodic oxidation using platinum as the cathode and the aluminum gate electrode as the anode. The anodic oxidation is effected by first increasing the voltage to 220 V at a constant rate, and then holding the voltage at 220 V for 1 hour to complete the oxidation. In case a constant current is applied as in the present case, the voltage is preferably increased at a rate of from 2 to 5 V/minute. An anodic oxide 109 is formed at a thickness of from 1,500 to 3,500 Å, more specifically, at a thickness of, for example, 2,000 Å in this manner (Fig. 6B).

[0079] Impurities (specifically in this case, phosphorus) are implanted into the island-like silicon film of the TFT in a self-aligned manner by ion doping (plasma doping) using the gate electrode portion as a mask. Phosphine (PH_3) is used as a doping gas to implant phosphorus at a dose of from 1×10^{15} to 4×10^{15} cm^{-2}.

[0080] The crystallinity of the portion whose crystallinity is impaired by the introduction of impurities is cured by irradiating a laser beam using a KrF excimer laser operating at a wavelength of 248 nm and a pulse width of 20 nsec. The laser is operated at an energy density of from 150 to 400 mJ/cm^2, preferably, in a range from 200 to 250 mJ/cm^2. Thus are formed N-type impurity regions (regions doped with phosphorus) 108. The sheet resistance of the regions is found to be in the range of 200 to 800 Ω/square.

[0081] This step of laser annealing can be replaced by an RTA process, i.e., a rapid thermal annealing process using a flash lamp, which comprises elevating the temperature of the silicon film rapidly to a range of from 1,000 to 1,200 °C (as measured on the silicon monitor). This method of annealing is also called as RTP (rapid thermal process).

[0082] A silicon oxide film is deposited thereafter to a thickness of 3,000 Å as an interlayer dielectric 110 by means of plasma CVD using TEOS together with oxygen, or by means of reduced pressure CVD or normal pressure CVD using TEOS together with ozone. The substrate temperature is maintained in the range of 250 to 450 °C, for instance, at 350 °C. A smooth surface is obtained thereafter by mechanically polishing the resulting silicon oxide film. An ITO coating is deposited thereon by sputtering, and is patterned to provide a pixel electrode 111 (Fig. 6D).

[0083] The interlayer dielectric 110 is etched to form contact holes in the source/drain as shown in Fig. 6E, and interconnections 112 and 113 are formed using chromium or titanium nitride to connect the interconnection 113 to the pixel electrode 111.

[0084] In the process according to the present invention, nickel is incorporated into the silicon film by using an aqueous solution containing nickel at such a low concentration of 10 ppm. Accordingly, a silicon film having a high resistance against hydrofluoric acid can be realized and contact holes can be formed stably and with high reproducibility.

[0085] A complete TFT can be formed by finally annealing the silicon film in hydrogen in a temperature

range of 300 to 400 °C for a duration of from 0.1 to 2 hours to accomplish the hydrogenation of the silicon film. A plurality of TFTs similar to the one described hereinbefore are fabricated simultaneously, and are arranged in a matrix to form an active matrix liquid crystal display device.

[0086] In accordance with the present example, the concentration of the nickel contained in the active layer is in the range of 5×10^{16} to 3×10^{18} atoms/cm^3.

[0087] As described above, the process according to the present example comprises crystallizing the portion into which nickel is introduced. However. the process can be modified as in Example 2. That is, nickel can be incorporated to selected portions through a mask, and crystals may be allowed to grow from the portions in a lateral direction. This region of crystal growth is used for the device. A device far more preferred from the viewpoint of electric stability and reliability can be realized by further lowering the nickel concentration of the active layer region of the device.

[Example 4]

[0088] This example is directed to a manufacture of a TFT used to control a pixel of an active matrix. Figs. 10A-10F are cross sectional views for explaining the manufacture of the TFT in accordance with this example.

[0089] Referring to Fig. 10A, a substrate 201, for example glass substrate, is washed and provided with a silicon oxide film 202 on its surface. The silicon oxide film 202 is formed through a plasma CVD with oxygen and tetraethoxysilane used as starting gases. The thickness of the film is 2000 Å, for example. Then, an amorphous silicon film 203 of an intrinsic type having a thickness of 500 - 1500 Å, for example, 1000 Å is formed on the silicon oxide film 202, following which a silicon oxide film 205 of 500 - 2000 Å, for example 1000 A is formed on the amorphous silicon film successively. Further, the silicon oxide film 205 is selectively etched in order to form an opening 206 at which the amorphous silicon film is exposed.

[0090] Then, a nickel containing solution (an acetic acid salt solution here) is coated on the entire surface in the same manner as set forth in Example 2. The concentration of nickel in the acetic acid salt solution is 100 ppm. The other conditions are the same as in Example 2. Thus, a nickel containing film 207 is formed.

[0091] The amorphous silicon film 203 provided with the nickel containing film in contact therewith is crystallized through a heat annealing at 500 - 620 °C for 4 hours in a nitrogen atmosphere. The crystallization starts from the region under the opening 206 where the silicon film directly contacts the nickel containing film and further proceeds in a direction parallel with the substrate. In the figure, a reference numeral 204 indicates a portion of the silicon film where the silicon film is directly added with nickel and crystallized while a reference numeral 203 indicates a portion where the crystal grows in a lateral direction. The crystals grown in the lateral direction are about 25 μm. Also, the direction of the crystal growth is approximately along an axes of [111].

[0092] After the crystallization, the silicon oxide film 205 is removed. At this time, an oxide film formed on the silicon film in the opening 206 is simultaneously removed. Further, the silicon film 204 is patterned by dry etching to form an active layer 208 in the form of an island as shown in Fig. 10B. It should be noted that the nickel is contained in the silicon film at a higher concentration not only under the opening 206 where the nickel is directly added but also at a portion where top ends of the crystals exist. The patterning of the silicon film should be done in such a manner that the patterned silicon film 208 should not include such portions at which nickel is contained at a higher concentration.

[0093] The patterned active layer 208 is then exposed to an atmosphere containing 100 % aqueous vapor of 10 atm at 500 - 600 °C, typically, 550 °C for one hour in order to oxidize the surface thereof and thus to form a silicon oxide film 209 of 1000 Å. After the oxidation, the substrate is maintained in an ammonium atmosphere (1 atm, 100 %) at 400 °C. At this condition, the silicon oxide film 209 is irradiated with an infrared light having an intensity peak at a wavelength in the range of 0.6 - 4 μm, for example, 0.8 - 1.4 μm for 30 - 180 seconds in order to nitride the silicon oxide film 209. HCl may be added to the atmosphere at 0.1 to 10 %. A halogen lamp is used as a light source of the infrared light. The intensity of the IR light is controlled so that a temperature on the surface of a monitoring single crystalline silicon wafer is set between 900 - 1200 °C. More specifically, the temperature is monitored by means of a thermocouple embedded in a single crystal silicon wafer and is transferred back to the IR light source (feed back). In the present example, the temperature rising rate is kept constant in the range of 50 - 200 °C/sec. and also the substrate is cooled naturally at 20 - 100 °C/sec. Since the IR light can heat the silicon film selectively, it is possible to minimize the heating of the glass substrate.

[0094] Referring to Fig. 10C, an aluminum film is formed by sputtering method to a thickness of 3000 - 8000 Å, for example, 6000 Å and then patterned into a gate electrode 210. The aluminum film may preferably contain scandium at 0.01 - 0.2 %.

[0095] Referring to Fig. 10D, the surface of the aluminum electrode 210 is anodic oxidized to form an anodic oxide film 211 in an ethylene glycol solution containing a tartaric acid at 1 - 5 %. The thickness of the oxide film 211 is 2000 Å, which will determine the size of an offset gate area which is to be formed in a later step as discussed below.

[0096] Referring then to Fig. 10E, using the gate electrode and the surrounding anodic oxide film as a mask, an N-type conductivity impurity (phosphorous, here) is introduced into the active layer in a self-aligning manner by ion doping method (also called as plasma doping

method) in order to form impurity regions 212 and 213. Phosphine (PH_3) is used as a dopant gas. The acceleration voltage is 60 - 90 kV, for example, 80 kV. The dose amount is 1×10^{15} - 8×10^{15} cm^{-2}, for example, 4×10^{15} cm^{-2}. As can be seen in the drawing, the impurity regions 212 and 213 are offset from the gate electrode by a distance "x". This configuration is advantageous for reducing a leak current (off current) which occurs when applying a reverse bias voltage (i.e. a negative voltage in the case of an NTFT) to the gate electrode. In particular, since it is desired that electric charges stored in a pixel electrode be maintained without leaking in order to obtain an excellent display, the offset configuration is particularly advantageous when the TFT is used for controlling a pixel of an active matrix as is the case in the present example.

[0097] Thereafter, an annealing is performed with a laser irradiation. As a laser, a KrF excimer laser (wavelength: 248 nm, pulse width: 20 nsec.) or other lasers may be used. The conditions of the laser irradiation in the case of KrF excimer laser are: energy density is 200 - 400 mJ/cm^2, for example, 250 mJ/cm^2, a number of shots is 2 - 10 shots per one site, for example, 2 shots. Preferably, the substrate is heated to 200 - 450 °C to enhance the effect of the irradiation.

[0098] Referring to Fig. 10F, an interlayer insulating film 214 of silicon oxide is formed through a plasma CVD to a thickness of 6000 Å. Further, a transparent polyimide film 215 is formed by spin coating to obtain a leveled surface. Then, a transparent conductive film made of indium tin oxide for example is formed on the leveled surface by sputtering to a thickness of 800 Å and patterned into a pixel electrode 216.

[0099] The interlayer insulating films 214 and 215 are provided with contact holes therethrough, through which electrode/wirings 217 and 218 can reach the impurity regions of the TFT. The electrode/wirings 217 and 218 are formed of a metallic material, for example, a multilayer of titanium nitride and aluminum. Finally, an annealing in a hydrogen atmosphere of 1 atm is carried out at 350 °C for 30 minutes in order to complete a pixel circuit of an active matrix circuit having TFTs.

[Example 5]

[0100] This example is directed to a manufacture of a TFT and will be described with reference to Figs. 11A - 11D. The same reference numerals will be referred to for describing the same or similar elements as those of the previous example.

[0101] Referring to Fig. 11A, a base film 202 of silicon oxide is initially formed on a Corning 7059 substrate 201 by sputtering to 2000 Å thick. The substrate is annealed at a temperature higher than a distortion point of the substrate following which the glass is cooled to a temperature less than the distortion point at a rate of 0.1 - 1.0 °C/minute. Thereby, it is possible to reduce a contraction of the substrate due to a substrate heating which occurs later (for example, thermal oxidation, thermal annealing), as a result, a mask alignment process will be facilitated. This step may be performed either before or after the formation of the base film 201 or it may be done both before and after the formation of the base film 201. In the case of using the Corning 7059 substrate, the substrate may be heated at 620 - 660 °C for 1-4 hours, following which it is cooled at 0.1 - 0.3 °C and taken out from a furnace when the temperature decreases to 400 - 500 °C.

[0102] Then, an intrinsic (I-type) amorphous silicon film is formed to 500-1500 Å thick, for example, 1000 Å through plasma CVD. The amorphous silicon film is crystallized in the same manner as in Example 1. Therefore, the redundant explanation will be omitted. After the crystallization, the silicon film is patterned into an island form having a dimension of 10 - 1000 microns square. Accordingly, a crystalline silicon film 208 in the form of an island is formed as an active layer of a TFT as shown in Fig. 11A.

[0103] Referring to Fig. 11B, the surface of the silicon film is oxidized by exposing the surface to an oxidizing atmosphere to form an oxide film 209. The oxidizing atmosphere contains an aqueous vapor at 70 - 90 %. The pressure and the temperature of the atmosphere is 1 atm and 500 - 750 °C, typically 600 °C. The atmosphere is produced by a pyrogenic reaction from oxygen and hydrogen gases with a hydrogen/oxygen ratio being 1.5 - 1.9. The silicon film is exposed to the thus formed atmosphere for 3 - 5 hours. As a result, the oxide film 209 having a thickness of 500 - 1500 Å, for example, 1000 Å is formed. Since the surface of the silicon film is reduced (eaten) by 50 Å or more due to the oxidation, an effect of a contamination of the upper most surface of the silicon film does not extend to the silicon-silicon oxide interface. In other words, by the oxidation, it is possible to obtain a clean silicon-silicon oxide interface. Also, since the thickness of the silicon oxide film is two times as the thickness of the portion of the silicon film to be oxidized, when the silicon film is originally 1000 Å thick and the silicon oxide film obtained is 1000 Å, the thickness of the silicon film remaining after the oxidation is 500 Å.

[0104] Generally, the thinner a silicon oxide film (gate insulating film) and an active layer are, the higher a mobility is and the smaller an off current is. On the other hand, a preliminary crystallization of an amorphous silicon film is easier when its thickness is thicker. Accordingly, there was a contradiction in the crystallization process and electrical characteristics with respect to the thickness of the active layer. The present example advantageously solves this problem. That is, the amorphous silicon film having a larger thickness is initially formed so that a better crystalline silicon film can be obtained, following which the thickness of the silicon film is reduced by the oxidation, resulting in an improvement of characteristics of the active layer of a TFT. Moreover, an amorphous component or grain boundaries con-

tained in the crystalline silicon film tend to be oxidized during the thermal oxidation, resulting in a decrease in recombination centers contained the active layer.

[0105] After the formation of the silicon oxide film 209 through thermal oxidation, the substrate is annealed in a 100 % monoxide dinitrogen atmosphere at 1 atm and 600 °C for 2 hours.

[0106] Referring to Fig. 11C, a silicon containing 0.01 to 0.2 % phosphorous is deposited through low pressure CVD to 3000 - 8000 Å thick, for example, 6000 Å, and then patterned into a gate electrode 210. Further, using the gate electrode 210 as a mask, an N-type conductivity impurity is added into a portion of the active layer in a self-aligning manner by ion doping. Phosphine is used as a dopant gas. The doping condition is substantially the same as in the Example 4. The dose amount is, for example, 5×10^{15} cm^{-2}. Thus, N-type impurity regions 212 and 213 are formed.

[0107] Thereafter, an annealing is performed with a KrF excimer laser in the same manner as set forth in Example 4. The laser annealing may be replaced by a lamp annealing with a near infrared ray. The near infrared ray is absorbed by crystalline silicon more effectively than by amorphous silicon. Accordingly, the annealing with the near infrared ray is comparable with a thermal annealing at 1000 °C or more. On the other hand, it is possible to prevent the glass substrate from being detrimentally heated inasmuch as the near infrared ray is not so absorbed by the glass substrate. That is, although a far infrared ray can be absorbed by a glass substrate, visible or near infrared ray of which wavelength ranges from 0.5 - 4 μm are not so absorbed.

[0108] Referring to Fig. 11D, an interlayer insulating film 214 of silicon oxide is formed to 6000 Å thick by a plasma CVD. A polyimide may be used instead of silicon oxide. Further, contact holes are formed through the insulating film. Electrode/wirings 217 and 218 are formed through the contact holes by using a multilayer of titanium nitride and aluminum films. Finally, an annealing in a hydrogen atmosphere is conducted at 350 °C and 1 atm for 30 minutes. Thus, a TFT is completed.

[0109] The mobility of the thus formed TFT is 110 - 150 cm^2/Vs. The S value is 0.2 - 0.5 V/digit. Also, in the case of forming a P-channel type TFT by doping boron into source and drain regions, the mobility is 90 - 120 cm^2/Vs and the S value is 0.4 - 0.6 V/digit. The mobility in accordance with the present example can be increased by 20 % or more and the S value can be reduced by 20 % or more as compared with a case where a gate insulating film is formed by a known PVD or CVD.

[0110] Also, the reliability of the TFT in accordance with the present example is comparable to that of a TFT which is produced through a thermal oxidation at a temperature as high as 1000 °C.

[Example 6]

[0111] Fig. 12 shows an example of an active matrix type liquid crystal device in accordance with the present example.

[0112] In the figure, reference numeral 61 shows a glass substrate, and 63 shows a pixel area having a plurality of pixels in the form of a matrix each of which is provided with a TFT as a switching element. Reference numeral 62 shows peripheral driver region(s) in which driver TFTs are provided in order to drive the TFTs of the pixel area. The pixel area 63 and the driver region 62 are united on the same substrate 61.

[0113] The TFTs provided in the driver region 62 need to have a high mobility in order to allow a large amount of electric currents to pass therethrough. Also the TFTs provided in the pixel area 63 need to have a lower leak current property in order to increase a charge retention ability of pixel electrodes. For example, the TFTs manufactured in accordance with Example 3 are suitable as the TFTs of the pixel area 63.

[Example 7]

[0114] The present example is a modification of Example 1. That is, before forming a nickel acetate aqueous solution, a rubbing treatment is performed on a silicon oxide surface in order to form number of minute scratches there.

[0115] Referring to Fig. 13A, a Corning 7059 substrate 11 having a silicon oxide film as a base film 18 is provided. The silicon oxide film is formed by sputtering to a thickness of 2000 Å for example. On the silicon oxide film, an amorphous silicon film 12 is formed by plasma CVD to a thickness of 300 - 800 Å, for example, 500 Å. Subsequently, the surface of the amorphous silicon film is treated with a hydrofluoric acid in order to remove a contamination or a natural oxide formed thereon. After that, a silicon oxide film of 10 - 100 Å thick is formed by exposing the substrate in an oxygen atmosphere with the surface being irradiated with a UV light (not shown). The oxidation may be carried out with a hydrogen peroxide treatment or thermal oxidation.

[0116] Then, fine scratches (unevenness or irregularity) are formed on the silicon oxide film by a rubbing treatment as shown by reference numeral 17. The rubbing treatment is carried out with a diamond paste. However, a cotton cloth or a rubber may be used instead of diamond paste. It is desirable that scratches have a uniform direction, width and gap.

[0117] After the rubbing treatment, a film of nickel acetate is formed by spin coating in the same manner as in Example 1. The nickel acetate solution is absorbed by the scratches uniformly.

[0118] Referring to Fig. 13B, the amorphous silicon film is then furnace annealed at 550 °C for 4 hours in a nitrogen atmosphere like in Example 1. Thus, a crystalline silicon film is obtained. The grain sizes and orientation directions of the grains 19 in the thus obtained film are more uniform than that obtained in Example 1. The grains 19 are extended in one direction and have an ap-

proximately rectangular or ellipse shape or the like.

[0119] The dimension or number of scratches can be controlled by changing a density of the diamond paste. Since it is difficult to observe the scratches with a microscope, the rubbing condition is determined in such a manner that the size of grains or density of remaining amorphous silicon in the obtained crystalline silicon film can be maximized. In this example, the condition of the treatment is selected so that lengths of amorphous regions which remain after the crystallization be 1 μm or less, preferably, 0.3 μm or less.

[0120] In the case of Example 1 in which a rubbing treatment is not performed, there is a tendency that the nickel is not uniformly diffused and non-crystallized regions in the form of 1 -10 μm circles are observed. Accordingly, the rubbing treatment improves the uniformity of the obtained crystals.

[Example 8]

[0121] The present example is directed to a manufacturing process of TFTs for switching pixels of an active matrix in accordance with Example 7. Figs. 14A-14E are cross sectional views showing the manufacturing process.

[0122] Referring to Fig. 14A, a silicon oxide film 202 is formed by a plasma CVD to a thickness of 3000 Å on a substrate 201 made of Corning 7059 glass (10 cm square). Then, an amorphous silicon film 203 is formed by plasma CVD to a thickness of 300 - 1000 Å, for example, 500 Å on the silicon oxide film 202.

[0123] The thus formed amorphous silicon film is crystallized by the process as set forth in Example 7. After the thermal crystallization, a laser annealing is performed in order to improve the crystallinity with a Kr excimer laser (248 nm wavelength) having a power density 200 - 350 mJ/cm^2. As a result, amorphous components which remain in the crystalline silicon film are completely crystallized.

[0124] After the crystallization, the silicon film 203 is patterned into an island form silicon film 208 as shown in Fig. 14B. At this time, the location and the direction of the silicon island with respect to grain boundaries can be selected in such a manner as shown in Figs. 15A and 15B.

[0125] When an electric current of a TFT crosses grain boundaries, the grain boundaries function as a resistance. On the other hand, the electric current is easy to flow along grain boundaries. Accordingly, the electrical characteristics of a TFT is greatly influenced by the number and direction of the grains (grain boundaries) included in the channel region. For example, when there are a number of TFTs, a leak current property of each TFT varies depending upon the number and direction of the grains contained in the channel region thereof.

[0126] The above problem becomes serious when the size of the grains is approximately the same as the size of the channel or is smaller than that. When the channel is sufficiently larger than grains, this dispersion is averaged and is not observed significantly.

[0127] For example, if there is no grain boundary in the channel, it can be expected that the TFT has an electrical property which is the same as that of a single crystalline TFT. On the other hand, when grain boundaries extend through the island along a direction of a drain current, the leak current becomes larger. In contrast, when grain boundaries extend in a direction perpendicular to a direction of a drain current, the leak current becomes smaller.

[0128] When TFTs are arranged in such a manner that its drain current flows in a direction along the rubbing direction, since crystals lengthen along the rubbing direction, the number of grain boundaries included in a channel tends to be nonuniform and therefore the leak current is likely to disperse. Moreover, the intensity of the leak current becomes larger because the grain boundaries are aligned with the direction of the drain current as shown in Fig. 15A. On the other hand, as shown in Fig. 15B, if a drain current flows in a direction perpendicular to the rubbing direction, the off current property can be stabilized. This is because the width of the grains 19 are approximately constant and the number of grains existing in the channel region 26 can be made constant. In conclusion, it is desirable to arrange the active region 208 in such a way that a drain current of a TFT flows in a direction perpendicular to the direction of grain boundaries, i.e. the rubbing directions. Moreover, the rubbing treatment makes the size of crystal grains uniform, which results in that non-crystallized region can be epitaxially crystallized by a subsequent laser irradiation.

[0129] As shown in Fig. 14B, a silicon oxide film of 200 - 1500 Å thick, for example, 1000 Å thick is formed as a gate insulating film 209 through plasma CVD.

[0130] Then, an aluminum containing Si at 1 weight % or Sc at 0.1 to 0.3 weight % is sputter formed to 1000 Å to 3 μm, for example 5000 Å, following which it is patterned into a gate electrode 210. The aluminum electrode is then subjected to an anodic oxidation process using an ethylene glycol solution containing a tartaric acid at 1-3 %. The pH of the electrolyte is about 7. A platinum electrode is used as a cathode while the aluminum electrode is used as an anode. The voltage is increased with an electric current maintained constant until it reaches 220 V and then this condition is maintained for one hour. As a result, an anodic oxide film 211 is formed to a thickness of 1500 - 3500 Å, for example 2000 Å.

[0131] Referring to Fig. 14C, an impurity having one conductivity type (boron) is introduced into the silicon island through an ion doping method with the gate electrode 210 used as a mask in a self-aligning manner. Diborane (B_2H_6) is used as a dopant gas. The dose amount is 4-10 x 10^{15} cm^{-2}. The acceleration voltage is 65 kV. Thus, a pair of impurity regions (p-type) 212 and 213 are obtained.

[0132] Thereafter, the impurity regions 212 and 213 are activated by irradiating KrF excimer laser (248 nm wavelength, 20 nsec. pulse width). The energy density of the laser beam is 200 - 400 mJ/cm^2, preferably, 250-300 mJ/cm^2.

[0133] Referring to Fig. 14D, an interlayer insulating film 214 made of silicon oxide is formed through plasma CVD to a thickness of 3000 Å. Then, a contact hole is formed on the impurity region 212 (source) through the interlayer insulating film 214 and the gate insulating film 209 by etching. An aluminum film is then formed by sputtering and patterned to form a source electrode 217.

[0134] Referring to Fig. 14E, silicon nitride is deposited through plasma CVD to 2000 - 6000 Å as a passivation film 215. A contact hole is formed on the impurity region (drain) 213 through the passivation film 215, interlayer insulating film 214 and the gate insulating film 209 by etching. Finally, an indium tin oxide film (ITO) is formed into a pixel electrode 216. Thus, a pixel TFT is obtained.

[0135] While the present invention has been disclosed in preferred embodiments, it is to be understood that the scope of the present invention should not be limited to the specific examples of the embodiments. Various modifications may be made.

[0136] For example, the nickel containing film may be formed by using a nonaqueous solution such as alcohol. When using an alcohol, the solution may be directly formed on the amorphous silicon film without using an oxide film. Specifically, a nickel containing compound such as nickel acetyl acetonate may be dissolved by ethanol. This material can be decomposed during the heating for the crystallization because the decomposition temperature thereof is relatively low. The amount of the nickel acetyl acetonate is selected so that the concentration of the nickel in the solution is controlled to be 100 ppm. The nickel containing film can be obtained by coating the solution and then dried by a spin dry method at 1500 rpm for 1 minute. Also, since the contact angle of the alcohol is smaller than that of water, the amount of the solution used for forming the film may be smaller than in the case when a water solution is used. In this case, a drop of 2 ml with respect to 100 mm square is appropriate. The subsequent steps for forming the crystalline silicon may be entirely the same as those explained in the preferred embodiments.

[0137] For another example, an elemental nickel may be dissolved by an acid. That is, a nitric acid of 0.1 mol/l is used as an acid. Nickel powder is dissolved in this acid at 50 ppm.

Claims

1. A semiconductor device having at least one thin film transistor, said thin film transistor comprising:

   a glass substrate;
   a channel region comprising a crystalline semiconductor layer comprising silicon formed over said glass substrate;
   source and drain regions with said channel region interposed therebetween;
   a gate insulating film adjacent to said channel region; and
   a gate electrode adjacent to said gate insulating film,
   wherein said crystalline semiconductor layer has a [111] axis in parallel with a surface of said glass substrate.

2. A semiconductor device having at least one thin film transistor, said thin film transistor comprising:

   a glass substrate;
   a channel region comprising a crystalline semiconductor layer comprising silicon formed over said glass substrate;
   source and drain regions with said channel region interposed therebetween;
   a gate insulating film adjacent to said channel region; and
   a gate electrode adjacent to said gate insulating film,
   wherein a surface of said crystalline semiconductor layer has at least one of {110}, {123}, {134}, {235}, {145}, {156}, {257} and {167} planes but not a {111} plane.

3. A semiconductor device having at least one thin film transistor, said thin film transistor comprising:

   a glass substrate;
   a channel region comprising a crystalline semiconductor layer comprising silicon formed over said glass substrate;
   source and drain regions with said channel region interposed therebetween;
   a gate insulating film adjacent to said channel region;
   and a gate electrode adjacent to said gate insulating film,
   wherein a surface of said crystalline semiconductor layer has a {110} plane but not a {111} plane.

4. A semiconductor device having at least one thin film transistor, said thin film transistor comprising:

   a channel region comprising a plurality of silicon crystals formed on an insulating surface;
   source and drain regions with said channel region interposed therebetween;
   a gate insulating film adjacent to said channel region; and
   a gate electrode adjacent to said gate insulat-

ing film,
wherein each of said silicon crystals has a [111] axis in parallel with said insulating surface.

5. A semiconductor device having at least one thin film transistor, said thin film transistor comprising:

a channel region comprising a plurality of silicon crystals formed on an insulating surface;
source and drain regions with said channel region interposed therebetween;
a gate insulating film adjacent to said channel region; and
a gate electrode adjacent to said gate insulating film,
wherein each of said silicon crystals has at least one of {110}, {123}, {134}, {235}, {145}, {156}, {257} and {167} planes but not a {111} plane.

6. A semiconductor device having at least one thin film transistor, said thin film transistor comprising:

a channel region comprising a plurality of silicon crystals formed on an insulating surface;
source and drain regions with said channel region interposed therebetween;
a gate insulating film adjacent to said channel region; and
a gate electrode adjacent to said gate insulating film,
wherein each of said silicon crystals has a {110} plane but not a {111} plane.

7. A semiconductor device according to any preceding claim wherein said channel region contains a catalyst element for promoting crystallization at a concentration not higher than 1 x 10^{19} atoms/cm^3.

8. A semiconductor device according to claim 7 wherein said catalyst element is selected from the group consisting of nickel, palladium, platinum, copper, silver, gold, indium, tin, phosphorus, arsenic and antimony.

9. A semiconductor device according to any preceding claim wherein at least said channel region of said crystalline semiconductor layer contains hydrogen.

10. A semiconductor device according to any preceding claim wherein said channel region is formed over a glass substrate.

11. An active matrix display device having a plurality of thin film transistors formed on an insulating surface, each of said thin film transistors having a semiconductive active region comprising a crystalline silicon film formed on said insulating surface, wherein said crystalline silicon film contains a catalyst element which promotes a crystallization of an amorphous silicon film at a concentration not higher than 1 x 10^{19} atoms/cm^3.

12. An active matrix display device according to claim 11 wherein said crystalline silicon film includes crystals having {111} axes and a crystal growth direction of said crystalline silicon film is approximately aligned with {111} axes of said crystals.

13. An active matrix display device according to claim 11 or 12 wherein a surface of said silicon film has at least one of the planes expressed by {hk1} (h+k=1).

14. An active matrix display device according to claim 13 wherein the planes expressed by {hk1} are {110}, {123}, {134}, {235}, {145}, {156}, {257} and {167}.

15. A semiconductor device including an active region comprising a crystalline silicon film formed on a substrate, wherein a surface of said silicon film has at least one of {110}, {123}, {134}, {235}, {145}, {156}, {257} and {167} planes, and said crystalline silicon film contains a catalyst element which promotes a crystallization of an amorphous silicon film at a concentration not higher than 1 x 10^{19} atoms/cm^3.

16. A semiconductor device having a thin film transistor formed on an insulating surface of a substrate, said thin film transistor comprising:

a crystalline semiconductor layer comprising silicon formed on said insulating surface;
a channel region formed within said crystalline semiconductor layer; and
a gate electrode adjacent to said channel region with a gate insulating layer interposed therebetween;
wherein said crystalline semiconductor layer contains a catalyst which is capable of promoting a crystallization of an amorphous silicon at a concentration not higher than 1 x 10^{19} atoms/cm^3 and preferably within a range of 1 x 10^{16} to 1 x 10^{19} atoms/cm^{-3}, and said crystalline semiconductor layer comprises silicon crystals extending uniformly in one direction parallel with said insulating surface.

17. A semiconductor device including at least one selected from the group consisting of a thin film transistor, a diode and a photosensor, said semiconductor device having an active region comprising a crystalline silicon film formed on a substrate, wherein a surface of said silicon film has at least one of planes expressed by {hk1} (h+k=1), and said crystalline silicon film contains a catalyst element which promotes a crystallization of an amorphous silicon

film at a concentration not higher than 1 x 10^{19} atoms/cm^3.

18. An active matrix display device having a plurality of thin film transistors formed on an insulating surface, each of said thin film transistors comprising:

a semiconductor active region comprising crystalline silicon formed on said insulating surface;
a channel region formed within said semiconductor active region; and
a gate electrode formed over said channel region with a gate insulating layer therebetween,
wherein said crystalline silicon film contains a catalyst element for promoting a crystallization of an amorphous silicon film at a concentration not higher than 1 x 10^{19} atoms/cm^3.

19. A semiconductor device comprising:

an active region comprising a crystalline silicon film formed on a substrate,
a channel region formed within said active region; and
a gate electrode formed over said channel region with a gate insulating layer therebetween,
wherein a surface of said silicon film has a {110} plane but does not have a {111} plane, and
wherein said crystalline silicon film contains a catalyst element for promoting a crystallization of an amorphous silicon film at a concentration not higher than 1 x 10^{19} atoms/cm^3.

20. A semiconductor device having a thin film transistor formed on an insulating surface of a substrate, said thin film transistor comprising:

a crystalline semiconductor layer comprising silicon formed on said insulating surface;
a channel region formed within said crystalline semiconductor layer; and
a gate electrode over said channel region with a gate insulating layer interposed therebetween,
wherein said crystalline semiconductor layer contains a catalyst capable of promoting a crystallization of an amorphous silicon at a concentration not higher than 1 x 10^{19} atoms/cm^3, and said crystalline semiconductor layer comprises silicon crystals extending uniformly in one direction parallel with said insulating surface.

21. A semiconductor device comprising:

a crystalline semiconductor film comprising silicon crystals formed on an insulating surface of a substrate wherein said silicon crystals have {111} axis in parallel with said insulating surface,
where a concentration of a catalyst element contained in said crystalline semiconductor film for promoting crystallization of said silicon crystals is 1 x 10^{19} atoms/cm^3.

22. A semiconductor device comprising:

a crystalline semiconductor film comprising silicon crystals formed on an insulating surface of a substrate wherein said silicon crystals have {111} axis in parallel with said insulating surface and a surface of said crystalline semiconductor film does not have a {111} plane,
wherein a concentration of a catalyst element contained in said crystalline semiconductor film for promoting crystallization of said silicon crystals is 1 x 10^{19} atoms/cm^3 or lower.

23. A semiconductor device comprising:

a crystalline semiconductor film comprising silicon crystals formed on an insulating surface of a substrate wherein a surface of said crystalline semiconductor film has at least one of {110}, {123}, {134}, {235}, {145}, {156}, {257} and {167} planes but not a {111} plane,
wherein a concentration of a catalyst element contained in said crystalline semiconductor film for promoting crystallization of said silicon crystals is 1 x 10^{19} atoms/cm^3 or lower.

24. A device according to any of claims 16 to 23 wherein said silicon is single crystal.

25. A device according to any of claims 16 to 24 wherein said crystalline semiconductor film is hydrogenated.

26. A device according to any of claims 16 to 25 wherein said catalyst element is selected from the group consisting of nickel, palladium, platinum, copper, silver, gold, indium, tin, phosphorus, arsenic and antimony.

27. A device according to any of claims 16 to 25 wherein said catalyst element is selected from groups VIII, IIIb, IVb and Vb.

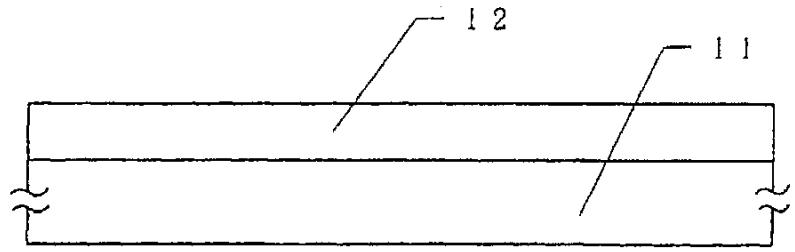


Fig.1A

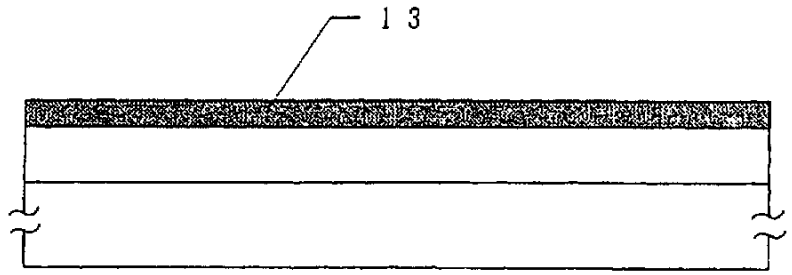


Fig.1B

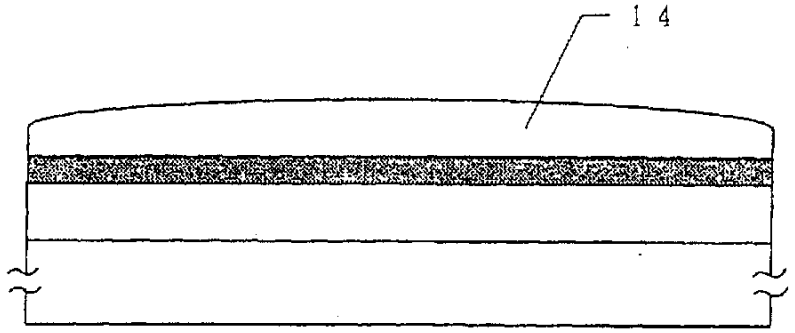


Fig.1C

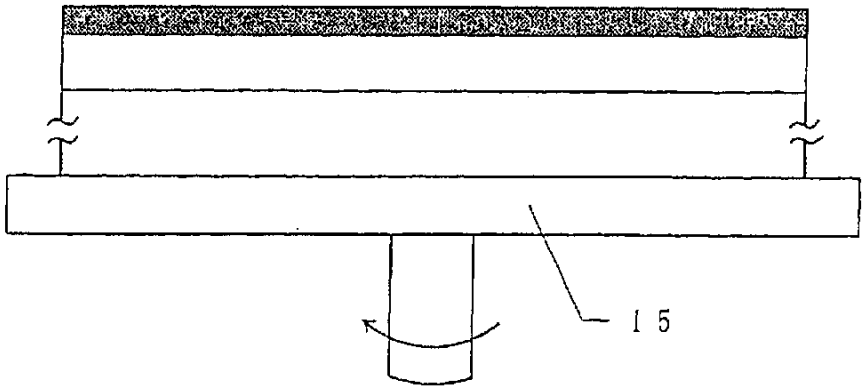


Fig.1D

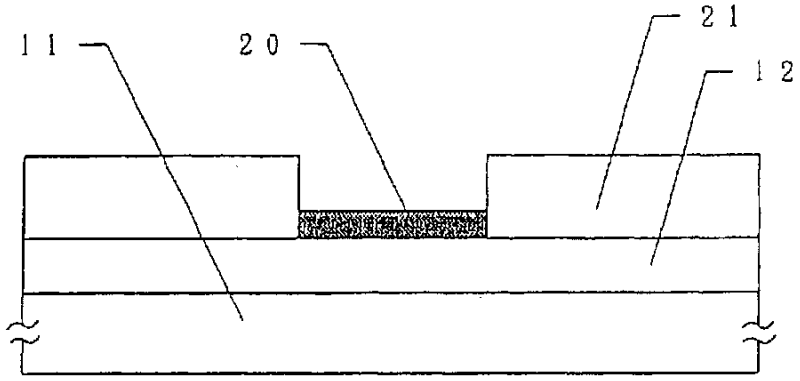


Fig. 2A

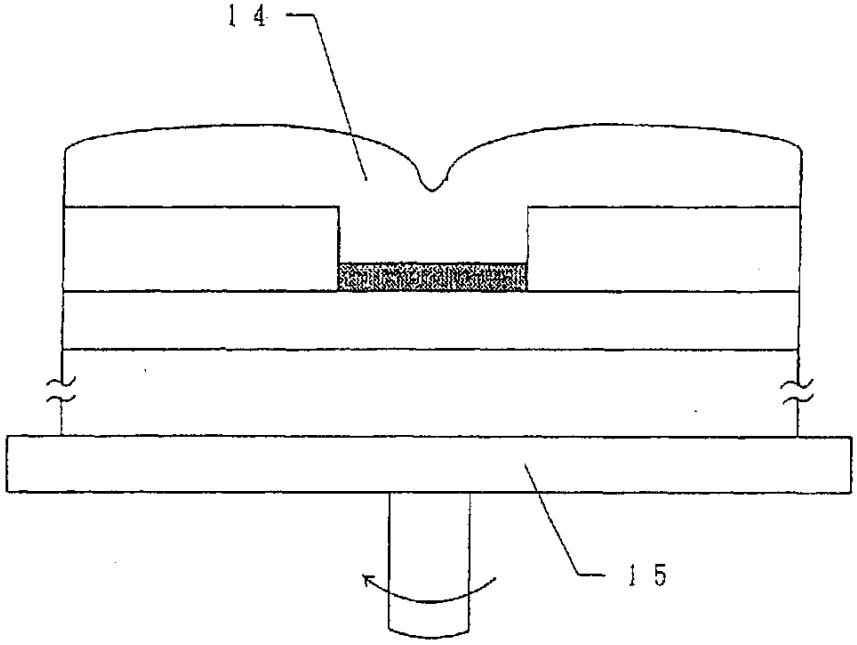


Fig. 2B

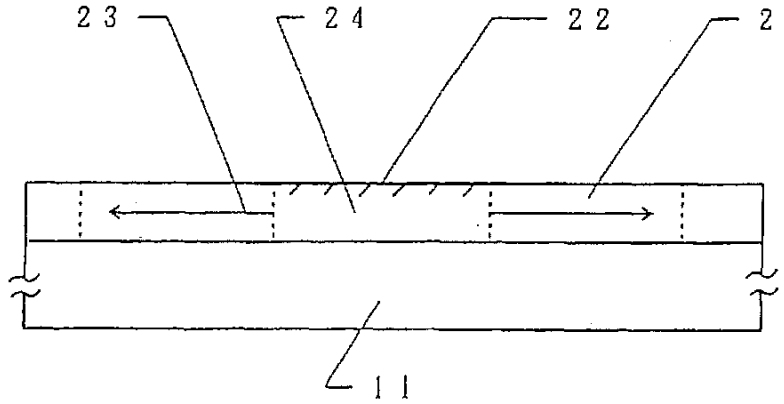


Fig. 2C

Fig. 3

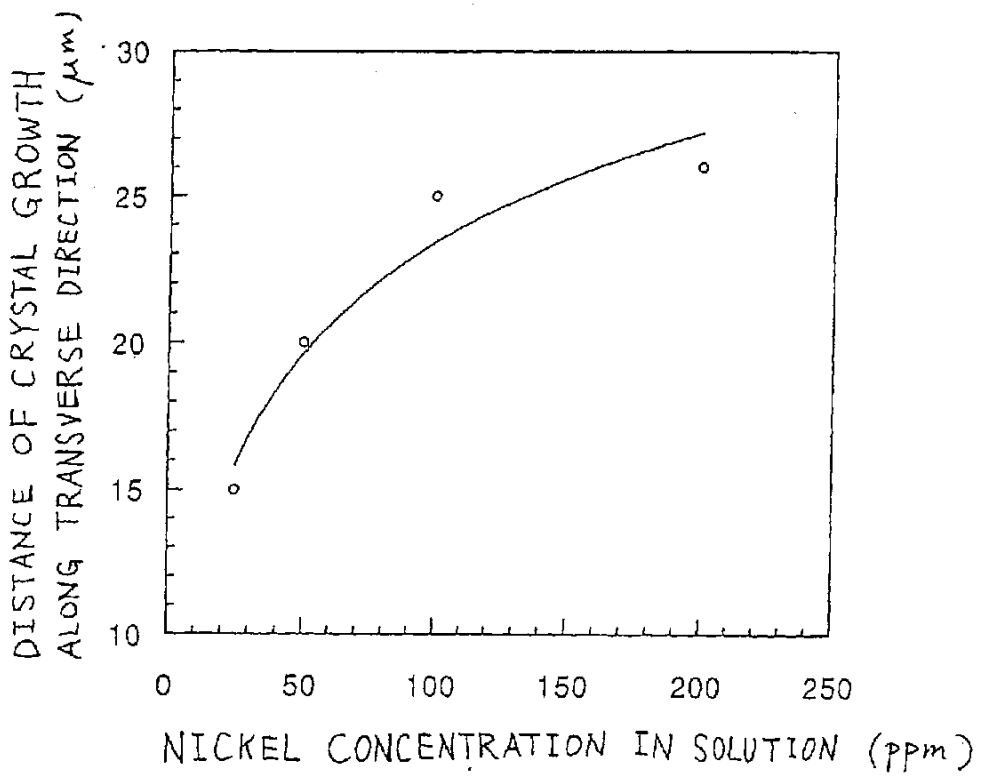

DISTANCE OF CRYSTAL GROWTH ALONG TRANSVERSE DIRECTION (μm)
30
25
20
15
10
0
50
100
150
200
250
NICKEL CONCENTRATION IN SOLUTION (ppm)

Fig.4

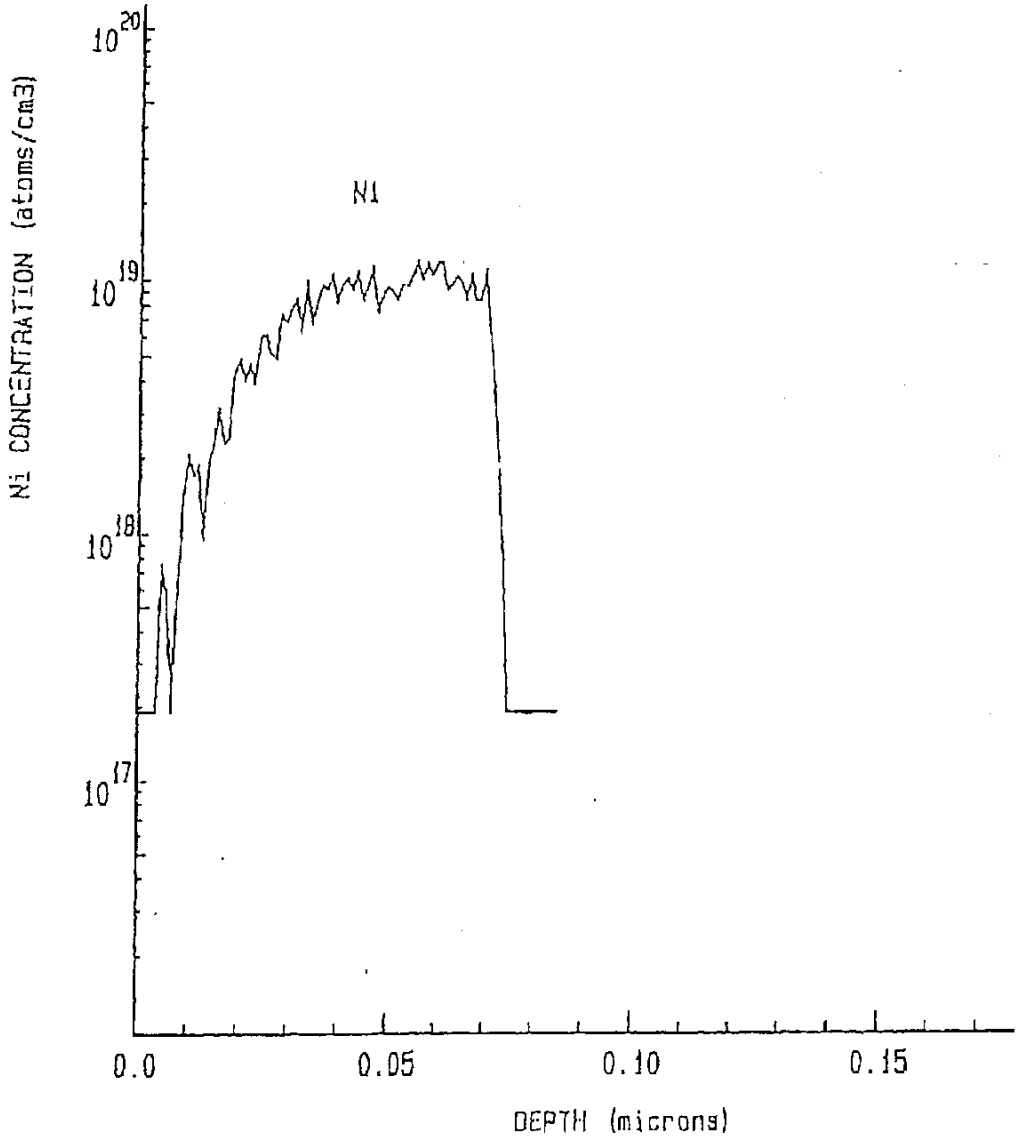
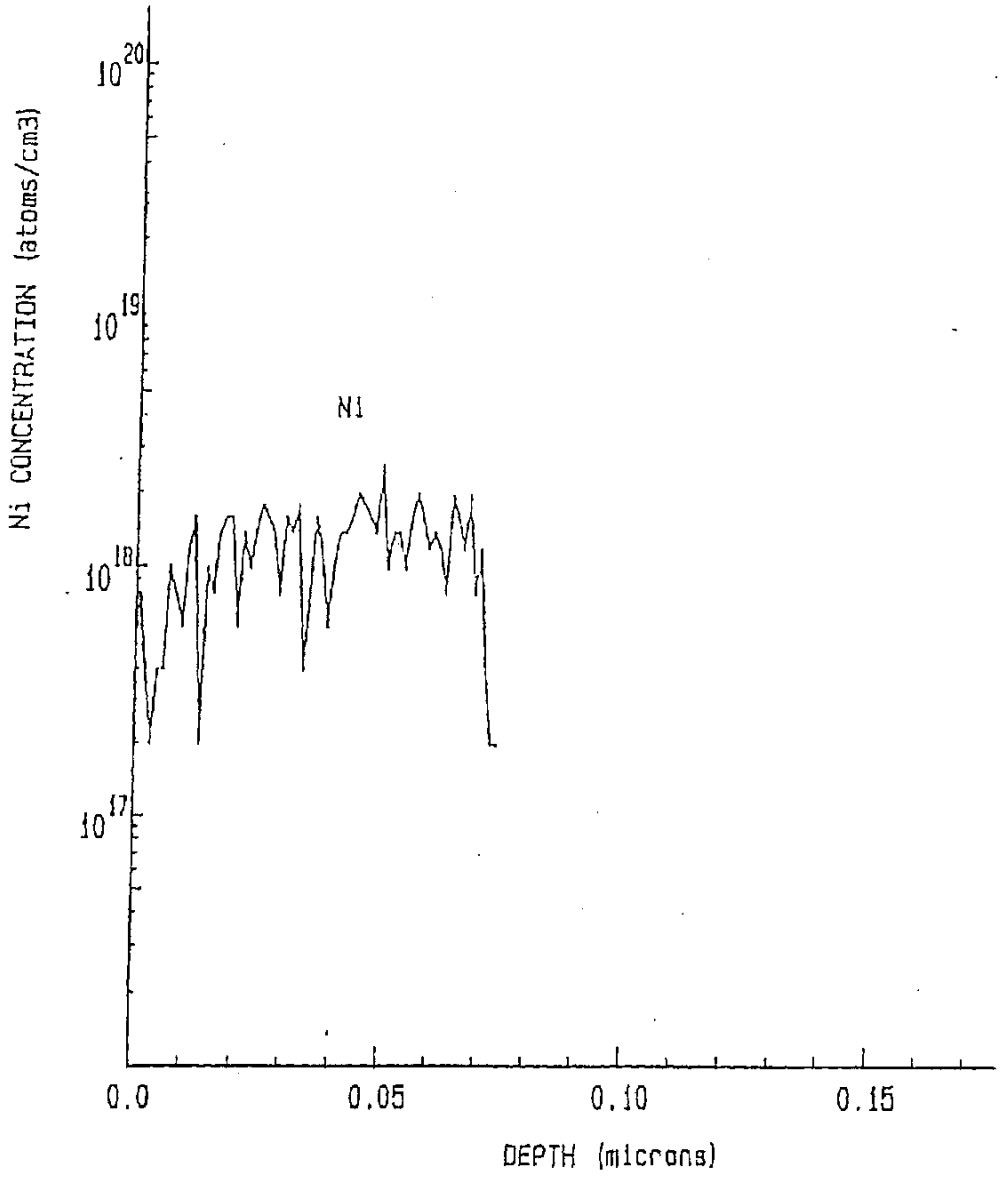

Ni CONCENTRATION (atoms/cm3)
10^20
10^19
10^18
10^17
Ni
0.0
0.05
0.10
0.15
DEPTH (microns)

Fig. 5


Ni CONCENTRATION (atoms/cm3)
10^20
10^19
10^18
10^17
Ni
0.0
0.05
0.10
0.15
DEPTH (microns)

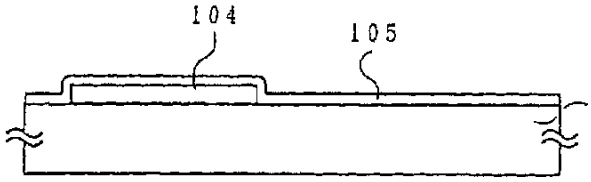


Fig. 6 A

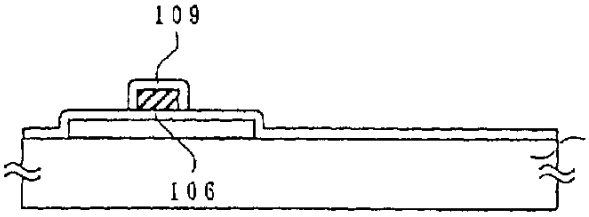


Fig. 6 B

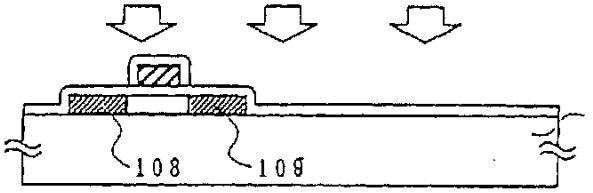


Fig. 6 C

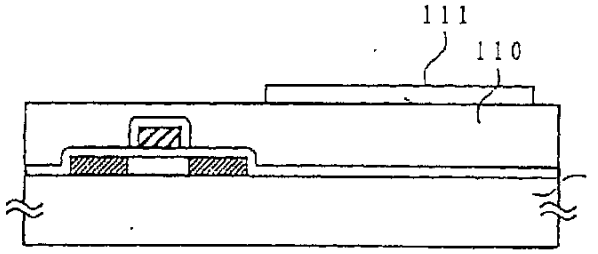


Fig. 6 D

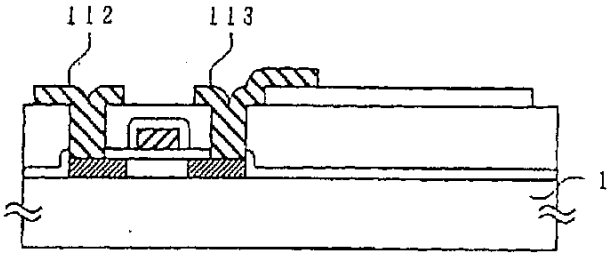


Fig. 6 E

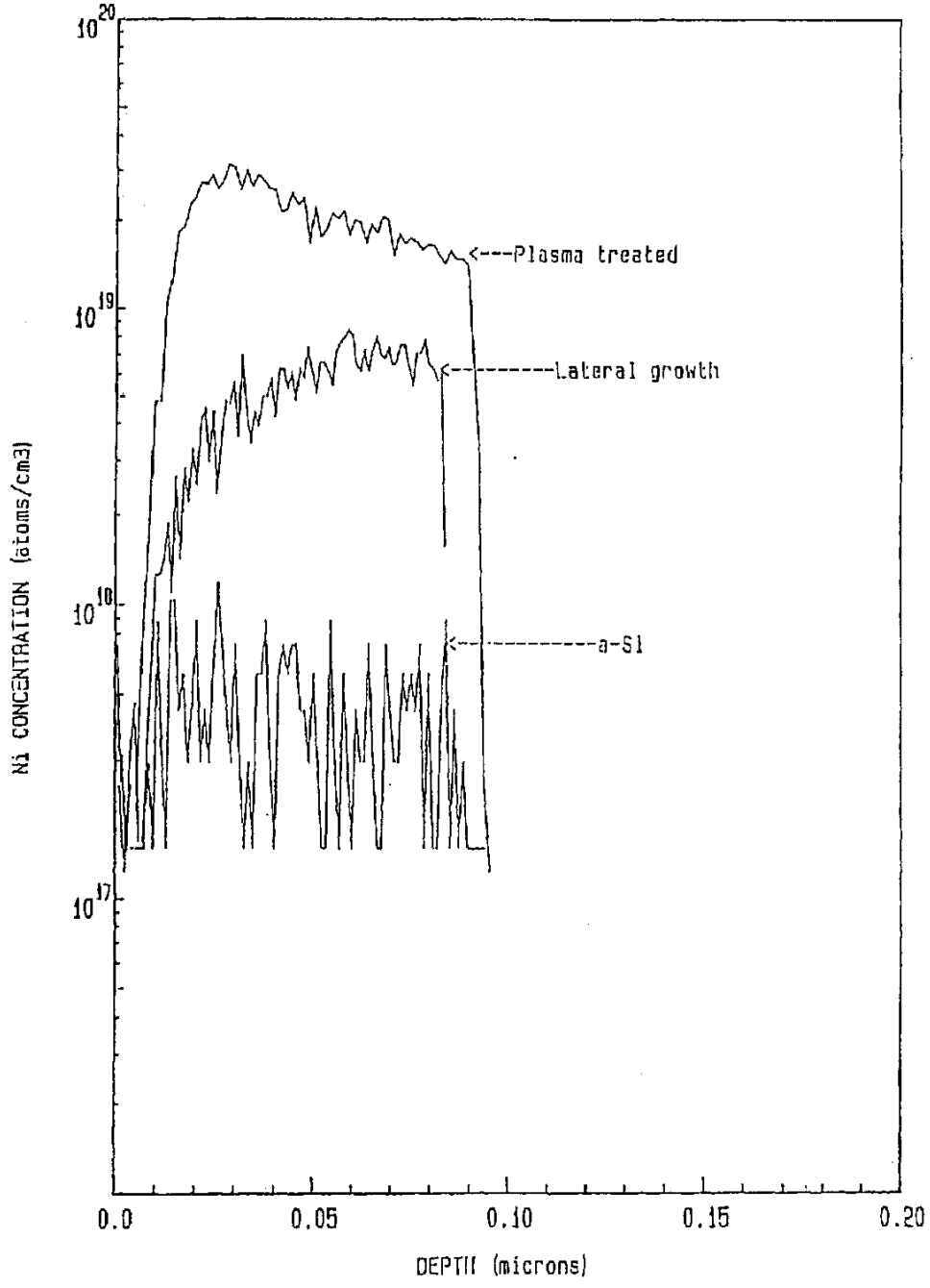

10^{20}
10^{19}
10^{18}
10^{17}
Ni CONCENTRATION (atoms/cm3)
<---Plasma treated
---------Lateral growth
----------a-Si
0.0
0.05
0.10
0.15
0.20
DEPTH (microns)

Fig. 7

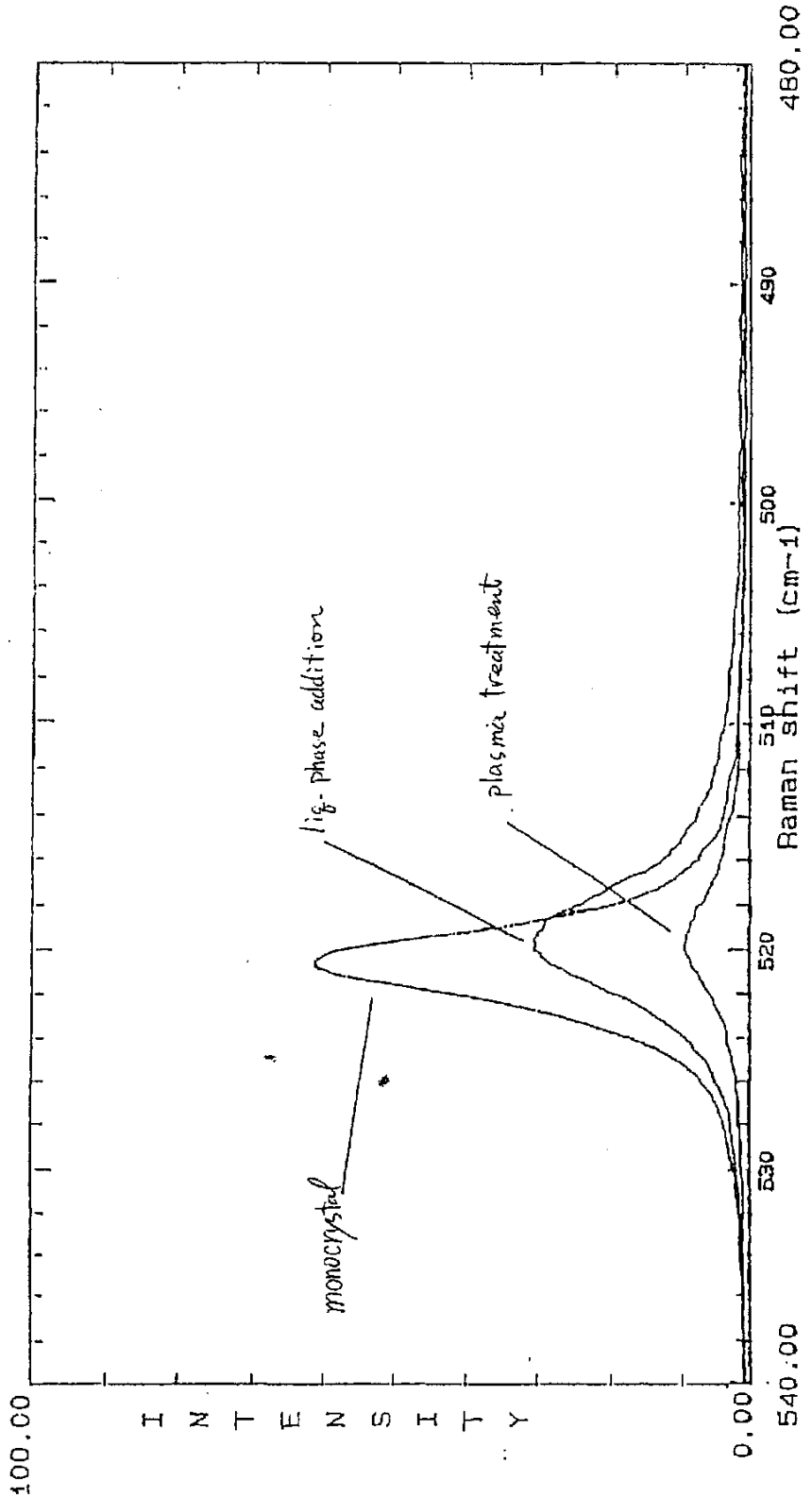

100.00
0.00
INTENSITY
540.00
530
520
510
500
490
480.00
Raman shift (cm-1)
liq. phase addition
plasma treatment
monocrystal

Fig. 8

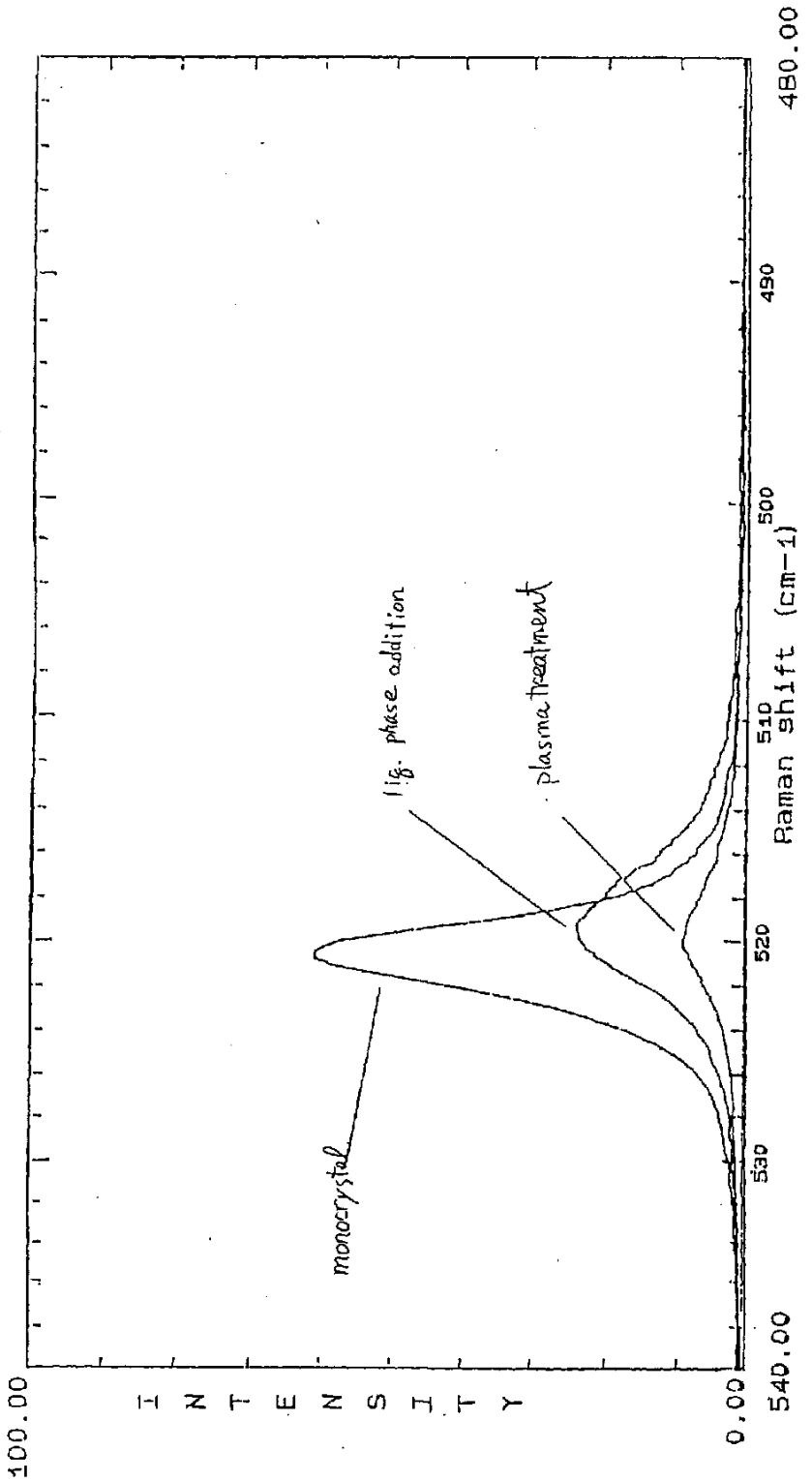

100.00
0.00
INTENSITY
540.00
480.00
490
500
510
520
530
Raman shift (cm-1)
monocrystal
liq. phase addition
plasma treatment

Fig. 9

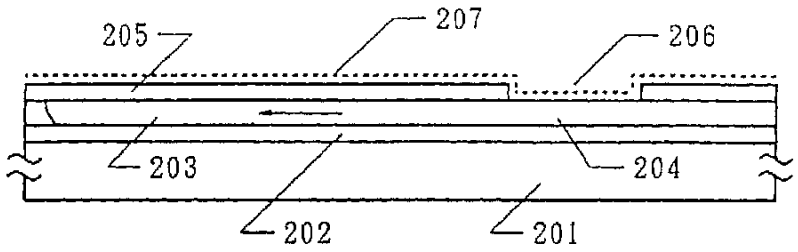


Fig. 10A

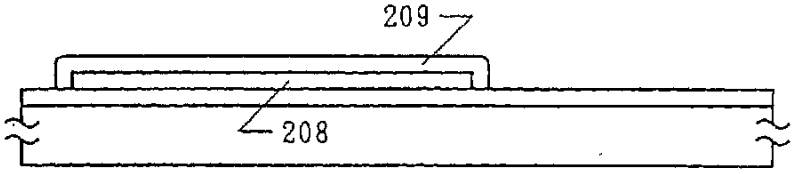


Fig. 10B

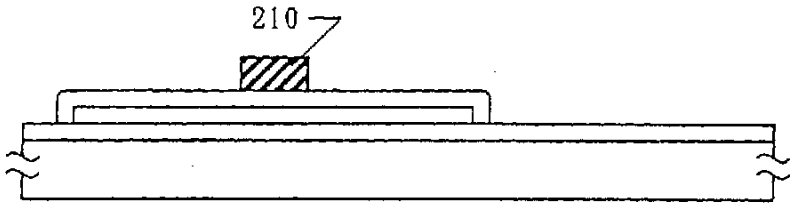


Fig. 10C

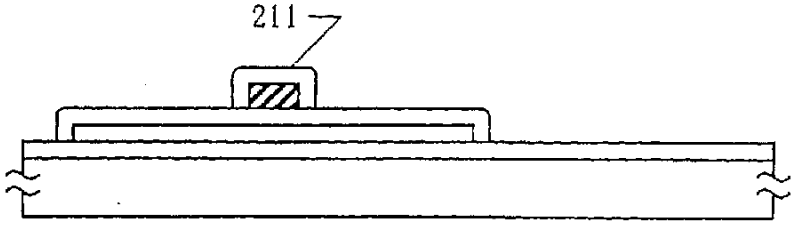


Fig. 10D

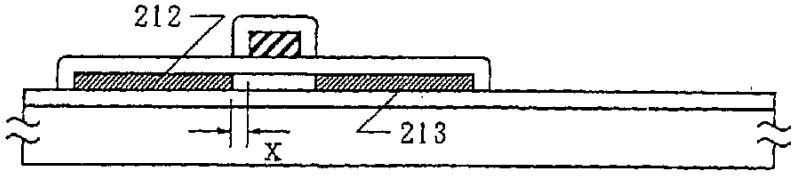


Fig. 10E

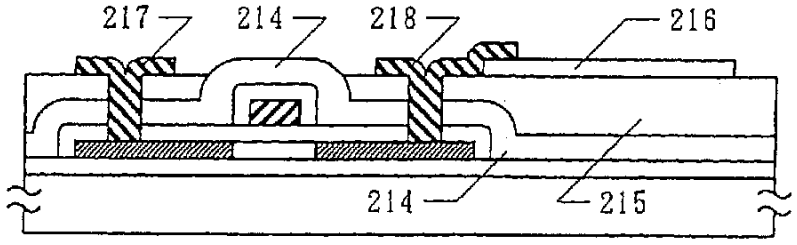


Fig. 10F

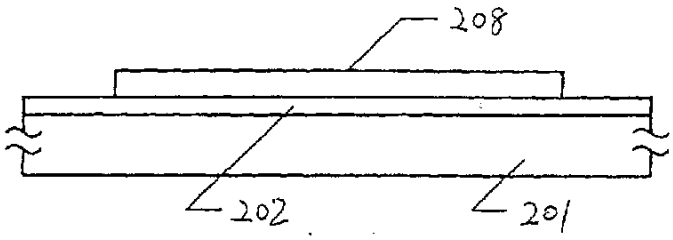


Fig. 11A

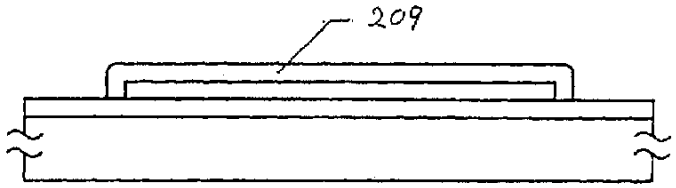


Fig. 11B

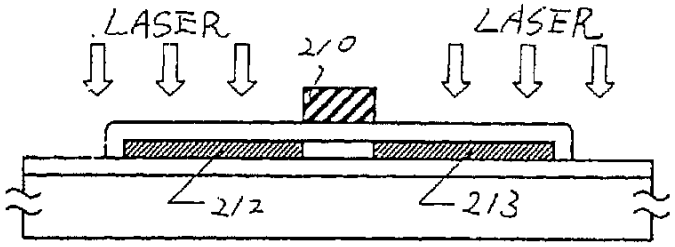


Fig. 11C

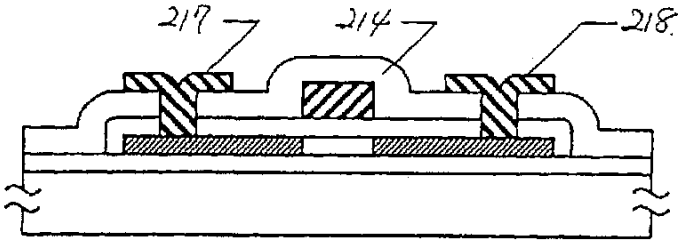


Fig. 11D

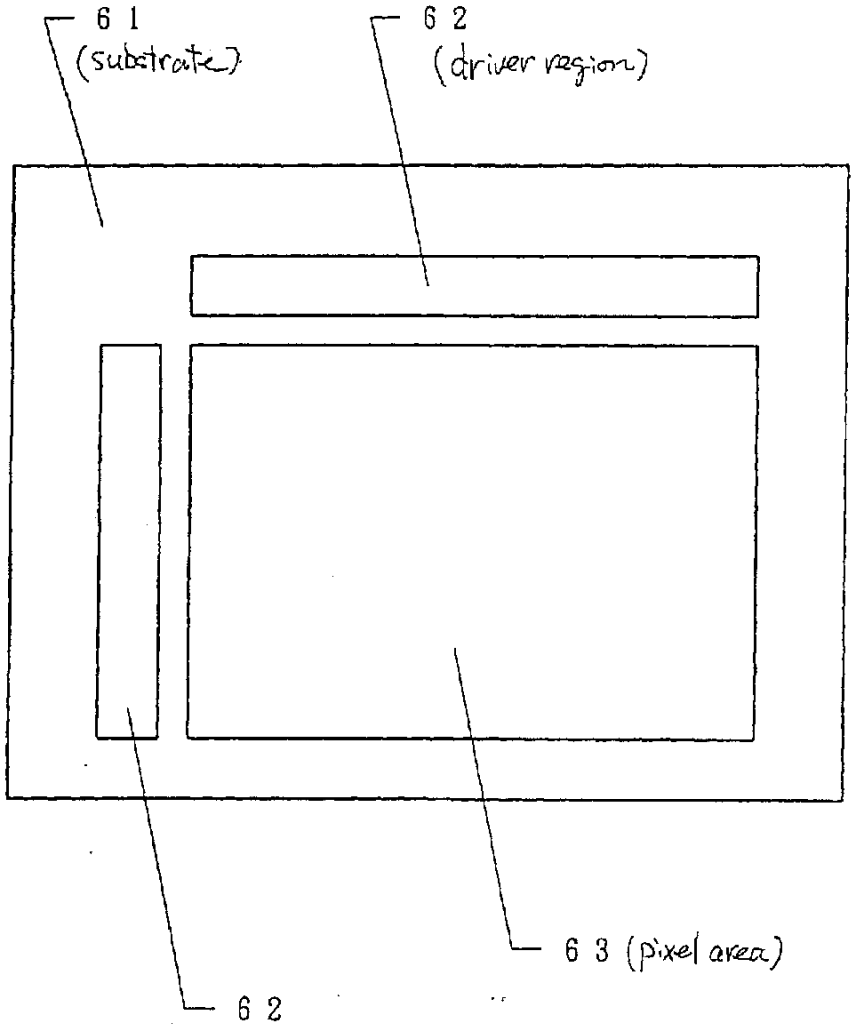


Fig. 12

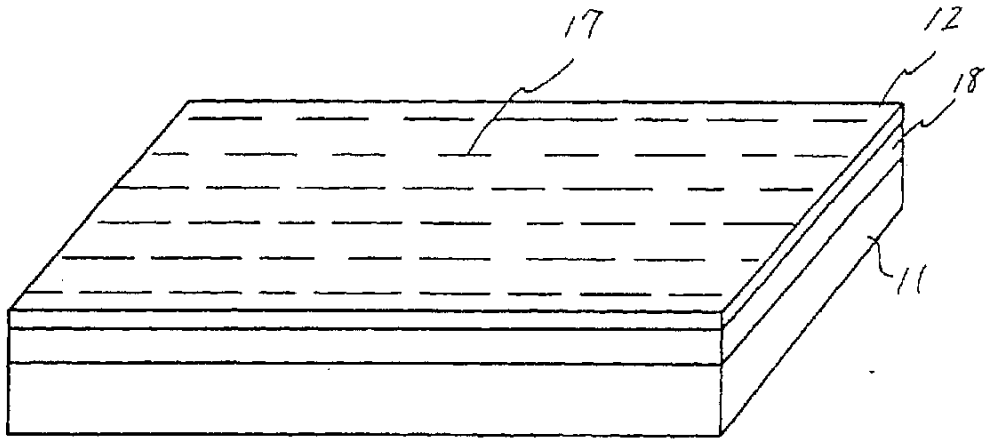


Fig. 13A

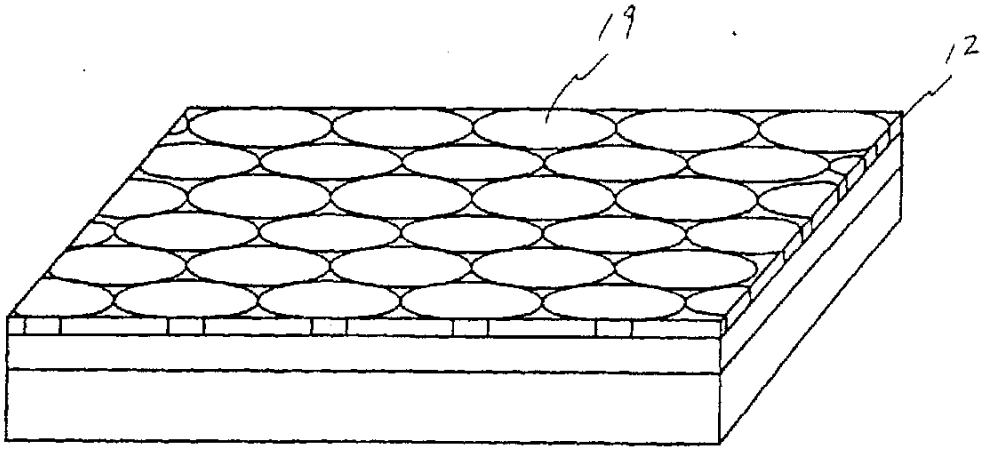


Fig. 13 B

Fig. 14 A

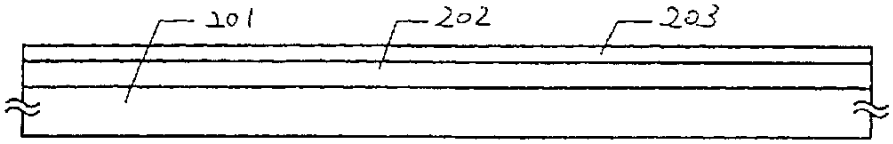


Fig. 14B

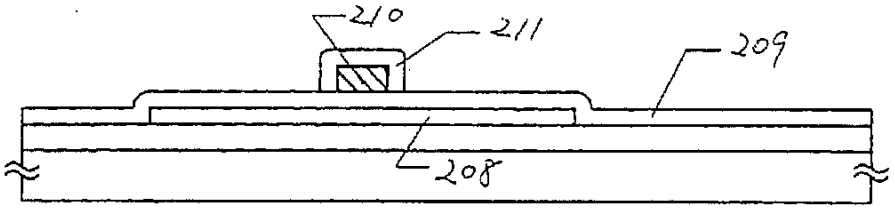


Fig. 14C

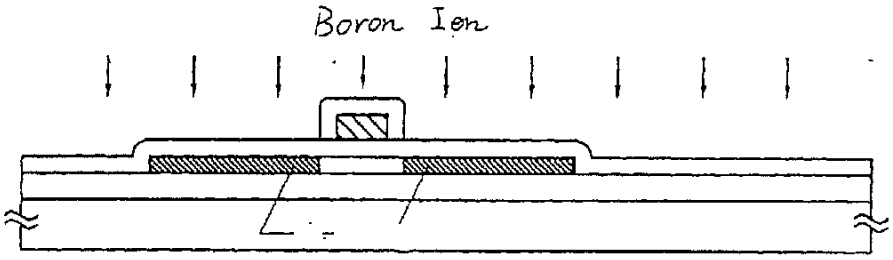


Fig. 14D

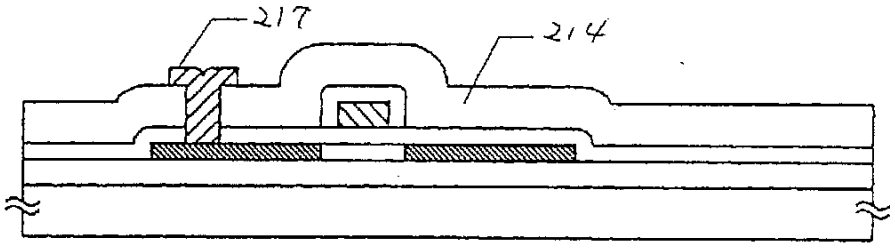
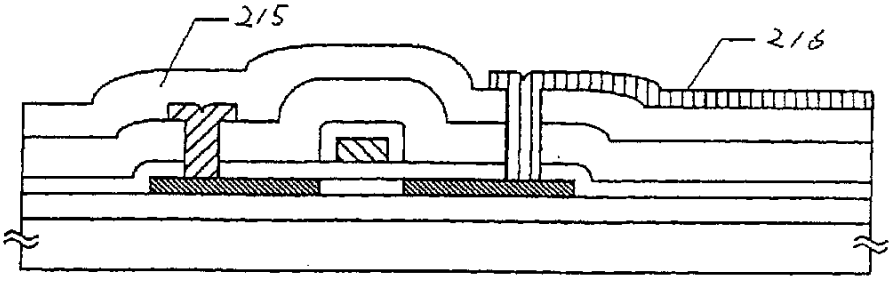


Fig. 14 E



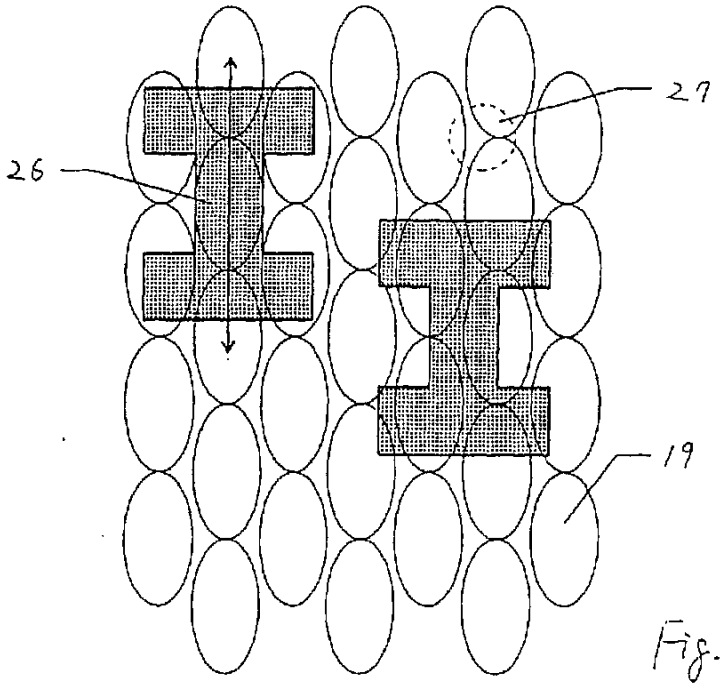


Fig. 15A

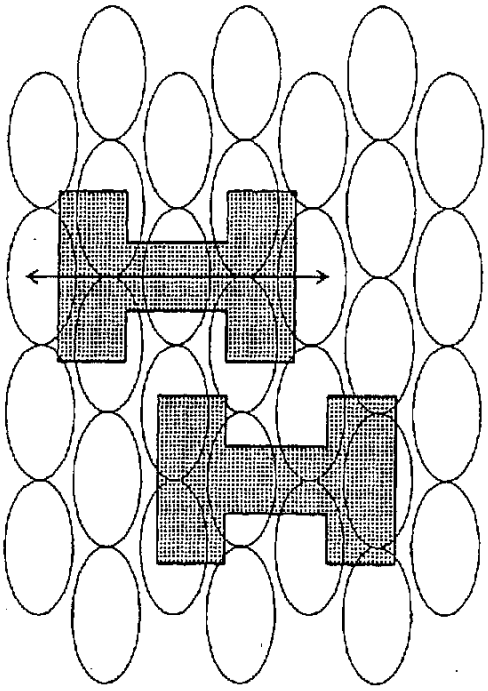


Fig. 15B

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European Patent Office
Office européen des brevets

(11) EP 1 158 580 A3

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(22) Date of filing: **31.10.1994**

(51) Int Cl.[7]: **H01L 21/84**, H01L 21/336, H01L 29/786

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09.11.1993 JP 30343693
12.11.1993 JP 30720693
20.06.1994 JP 16270594

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
94307986.3 / 0 651 431

(71) Applicant: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.**
Atsugi-shi Kanagawa-ken 243-0036 (JP)

(72) Inventors:
- **Ohtani, Hisashi**
  Isehara-shi, Kanagawa-ken 259-11 (JP)
- **Miyanaga, Akiharu**
  Hadano-shi, Kanagawa-ken 257 (JP)
- **Fukunaga, Takeshi**
  398 Hase Atsugi-shi, Kanagawa-ken, 243 (JP)
- **Zhang, Hongyong**
  398 Hase Atsugi-shi Kanagawa-ken, 243 (JP)

(74) Representative: **Milhench, Howard Leslie et al**
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

(54) Method of crystallizing a silicon layer

(57) A process for fabricating a highly stable and reliable semiconductor, comprising: coating the surface of an amorphous silicon film with a solution containing a catalyst element capable of accelerating the crystallization of the amorphous silicon film, and heat treating the amorphous silicon film thereafter to crystallize the film.

EP 1 158 580 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 11 6025

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 4 534 820 A (MORI HIDEFUMI ET AL) 13 August 1985 (1985-08-13) * column 7, line 21 - line 32 *	1,4, 7-10,21, 22	H01L21/84 H01L21/336 H01L29/786
A	US 4 801 351 A (MIYAJIMA TOSHIAKI ET AL) 31 January 1989 (1989-01-31) * figure 1 *	1,4, 7-10,21, 22	
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 387 (E-0967), 21 August 1990 (1990-08-21) & JP 02 143415 A (NIPPON SHEET GLASS CO LTD), 1 June 1990 (1990-06-01) * abstract *	1,4, 7-10,21, 22	
A	US 5 147 826 A (LIU GANG ET AL) 15 September 1992 (1992-09-15) * claim 1 *	1	
A	US 5 130 264 A (TROXELL JOHN R ET AL) 14 July 1992 (1992-07-14) * claim 1 *	1	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	WO 86/03621 A (AMERICAN TELEPHONE & TELEGRAPH) 19 June 1986 (1986-06-19) * figures 1-5 *	1	
P,A	EP 0 612 102 A (SEMICONDUCTOR ENERGY LAB) 24 August 1994 (1994-08-24) * figure 2 *	1	

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
Berlin	24 February 2004	Juhl, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 01 11 6025

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1,4,7-10,21,22

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 01 11 6025

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1,4,7-10,21,22

   TFT with [111] axis parallel to substrate surface

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2. claims: 2,3,5,6,15,17,19

   TFT with semiconductor layer having a {110}, {123},... surface

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3. claims: 11-14,16,18,20,23-27

   TFTs having catalyst elements at a concentration not higher than 1 x 10 exp 19 atoms/ccm.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 11 6025

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The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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